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MILITARY ADAPTATION OF COMMERCIAL ITEM (MACI) PROGRAM ON ELECTR--ETC(U)

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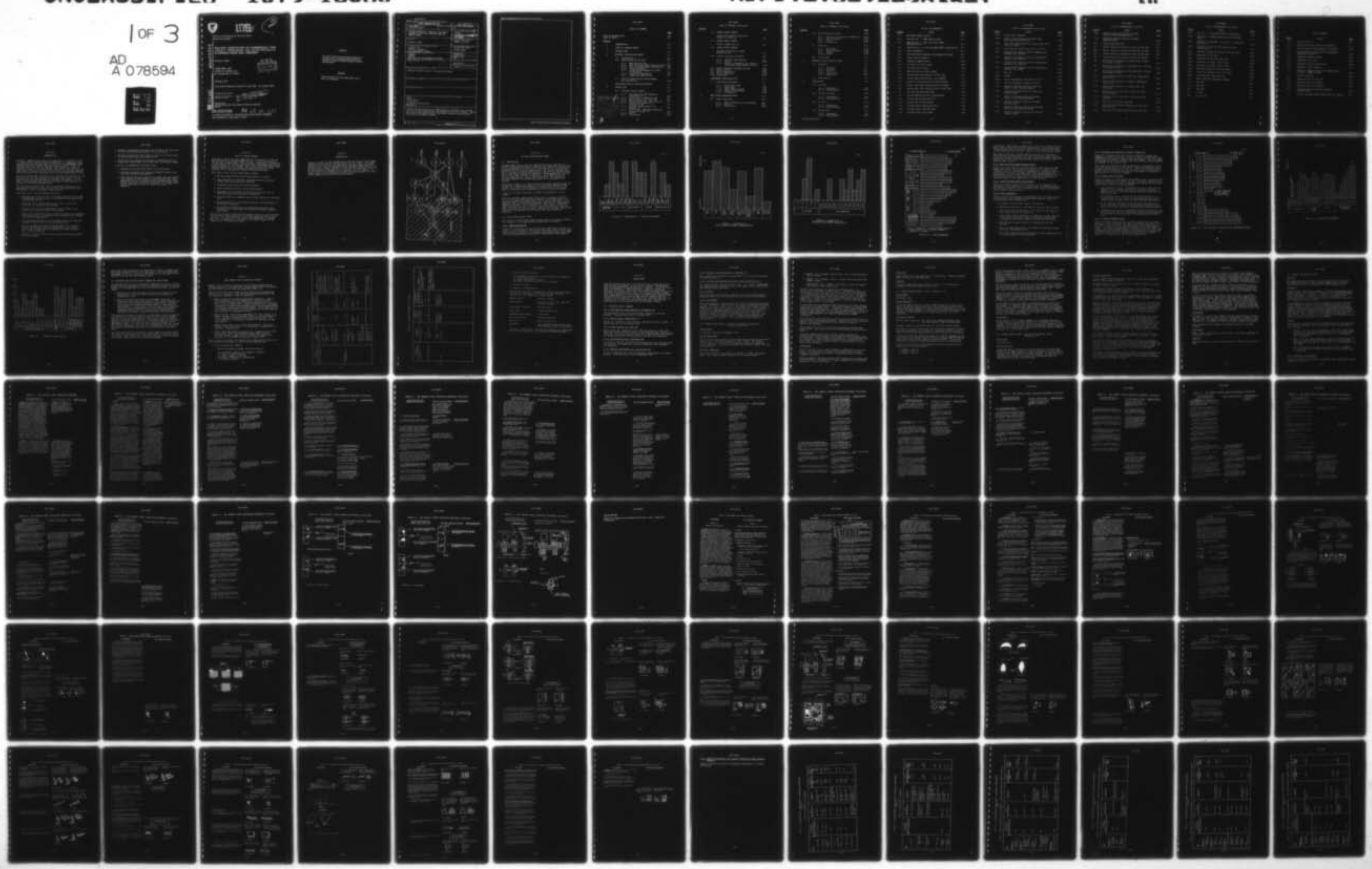

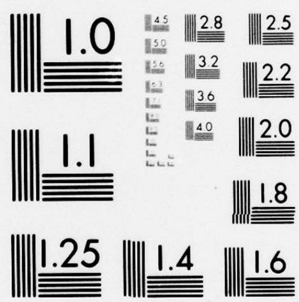
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Research and Development Technical Report
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MILITARY ADAPTATION OF COMMERCIAL ITEM (MACI) PROGRAM ON ELECTRICALLY ALTERABLE READ ONLY MEMORY

Richard L. Wiker

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October 1979

First Interim Report for period 15 July 1978 - 15 January 1979

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20. ABSTRACT (CONTINUE ON REVERSE SIDE IF NECESSARY AND IDENTIFY BY BLOCK NUMBER)

A miliary applications survey for EAROM devices was conducted. Three potential vendors of suitable EAROM devices were identified at GI, NCR and Nitron. Devices were procured and testing started. Measurement techniques were developed to characterize unique MNOS parameters.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

Section 1

INTRODUCTION

The MACI - EAROM Program (Military Adaptation of a Commercial Item for Electrically Alterable Read Only Memories) is designed to study commercially available MNOS Memory Devices of the EAROM/WAROM (Word Alterable Read Only Memory) type and determine which, if any, are suitable for use in military systems. The results will show (1) which device/devices are feasible for military use (2) the range and conditions of that use and its correlation to the expressed optimum device characteristics indicated by the military applications survey.

Due to the unique MNOS characteristics, and the fact that none of the available devices are specified to military range conditions, the objectives of the MACI program are different from others. In this case, a practical military specification must be developed which is suitable to the MNOS characteristics.

The well established MIL-883, Class B screening normally used for semiconductor devices is used for measuring those parameters which are similar to more conventional memory devices.

The objectives of the MACI-EAROM Program are:

a. Determine the range and type of military applications for MNOS EAROM/WAROMS and the features and parameters most significant in these applications.

b. Determine who is making MNOS devices, which devices are available and should be investigated.

c. Determine the status of MNOS memory device vendors, their support for these devices and future plans.

d. Develop test plans for, procure and functionally test candidate MNOS memory devices to determine their suitability for identified military applications.

e. Perform package studies on all candidate devices to determine mechanical suitability to military applications.

f. Perform a comparative study of the results of all previous testing and analysis and with ERADCOM concurrence select a device type or types which are optimum for future military slash sheet development.

g. Develop a screening test plan for the selected device/devices and procure parts.

h. Develop a preliminary slash sheet specification and test plan to verify device/devices against the specification.

i. Perform screening and slash sheet testing on sufficient parts to verify slash sheet and screening test.

j. Deliver 50 parts tested and screened to ERADCOM meeting the slash sheet requirements (50 of each type, if multiple types).

k. Deliver to ERADCOM the following items:

1. Prospective Military Slash Sheet of selected part.

2. Screening procedures for selecting commercial parts that will meet military requirements.

3. Final report detailing results of the MACI program, explanatory information not covered in specifications and recommendations for future programs involving MNOS and/or other memory technology (including information on new MNOS memory devices that mature after the selection process is complete).

Section 2

SCOPE OF INTERIM REPORT

This report covers the tasks completed for the majority of the pre-selection phase of the MACI/EAROM contract. Significant delays in the delivery of MNOS memory parts resulted in delaying the production of this report until useful, meaningful data development and analysis could contribute to its context. The current parts procurement delay problems appear not only in MNOS type memory devices but to be inherent in all semiconductor memory device procurements.

This report covers the following general tasks:

a. Military Applications Survey and analysis of results.

b. Data collection on potential candidate devices and device vendors and future potential analysis.

c. Candidate device selection and procurement.

d. Device packaging studies, pre-selection phase.

e. Development of preliminary characterization plans for all candidate devices and optimum test patterns.

f. Characterization of candidate devices and analysis of resultant data.

g. Characterization of unique MNOS parameters and development of measurement techniques.

h. Preliminary development of screening and slash sheet test procedures for unique MNOS and conventional memory parameter measurement.

Some testing results (primarily DC Parameter Tests) are not available at the time of this report due to internal scheduling and priority problems. The results of this testing and enhancement of present data and its analysis will be shown in the Phase I report on the completion of the projection phase.

Section 3

PROGRAM PLAN

Figure 3-1 shows the MACI/EAROM program and the portion of the tasks completed at the time of the publication of this report. The small portion of the test and characterization and most promising device selection that remains represents the DC Parameter Tests that are in progress and the final selection of the best device/devices that will be coordinated with ERADCOM at the completion of this report. It appears from early DC Parameter Testing that these results will have little impact on the device selection process.

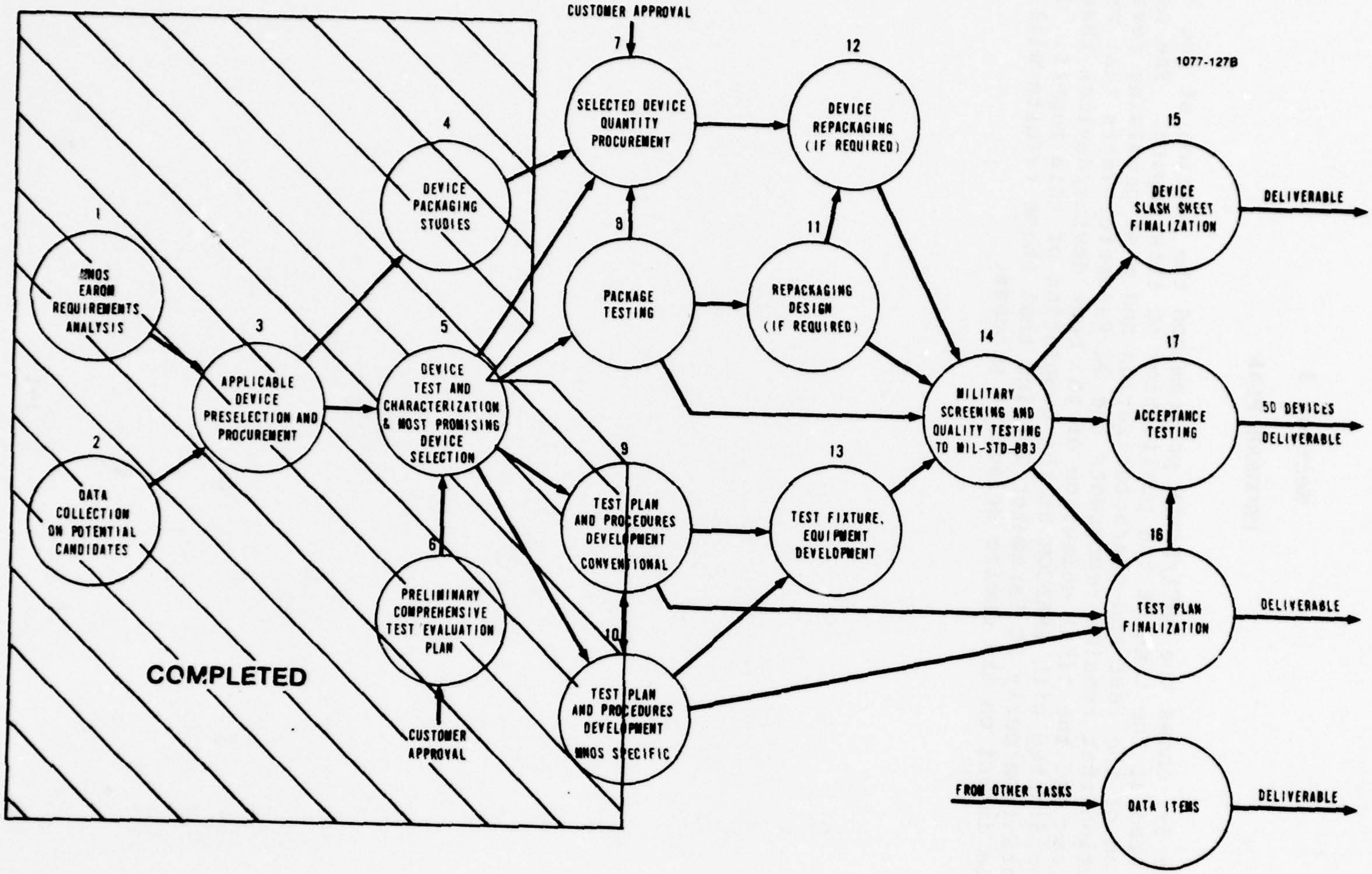


FIGURE 3-1. MACI-MNOS EAROM PROGRAM

Section 4

MILITARY APPLICATIONS SURVEY

4.1 INTRODUCTION

The MNOS Memory Device Military Applications Survey consists of a series of questions designed to determine the important criteria used by system designers in selecting or rejecting the use of nonvolatile memory devices in military applications. The survey questions were sent to selected technical people both within military organizations and in the defense contractor community. These people were selected due to their past, present, or potential use of MNOS devices in military applications. While only one-third of the surveys were returned, definite trends and preferences were indicated by the results.

The primary objective of these surveys was to help establish both the criteria for comparative judging of the available commercial MNOS devices and to aid in determining the optimum type of tests to be used, to establish their suitability for use in military systems.

A copy of the survey questions is shown in Attachment A to this report.

While the Military Applications Survey was in progress, the early results and background knowledge gained by use of MNOS devices in military systems at Honeywell were used to develop the Task I report (MNOS Devices for Military and Aerospace Applications) submitted to ERADCOM in November 1978 (Attachment B). This report illustrates some configurations used in military applications both in the read mostly and data acquisition modes. The data in the Task I Report and Application Surveys was used to develop the device selection criteria.

4.2 APPLICATIONS SURVEY DATA

The results of the Military Applications Survey are shown in Figures 4-1 through 4-4 with appropriate explanations interspersed.

4.2.1 MNOS Applications

Figure 4-1 illustrates the prime areas where MNOS memory devices are being or will be applied. The significant points apparent from these results indicate primary use in special environment large store memories and microcomputer/microcontroller applications where speed is

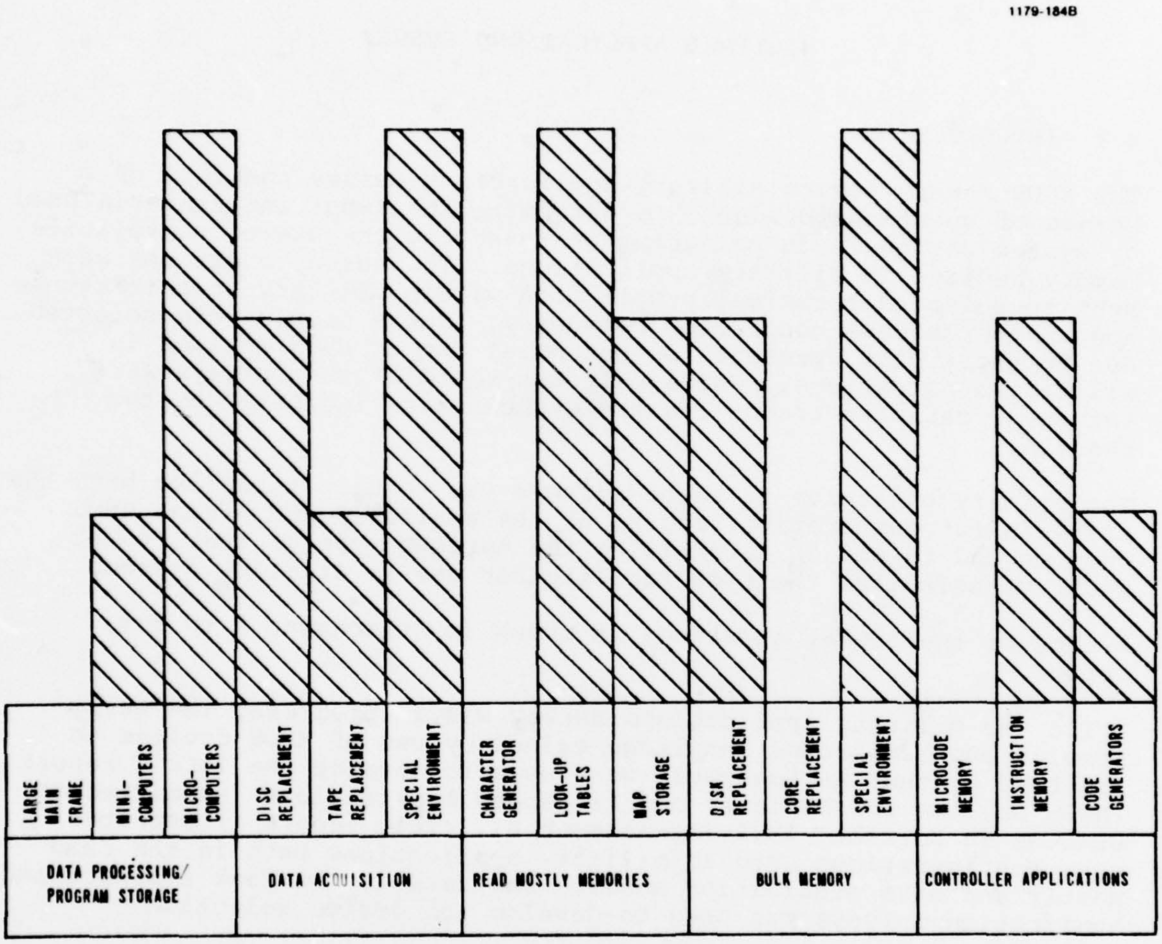


FIGURE 4-1. QUESTION NO. 2 - MNOS APPLICATIONS

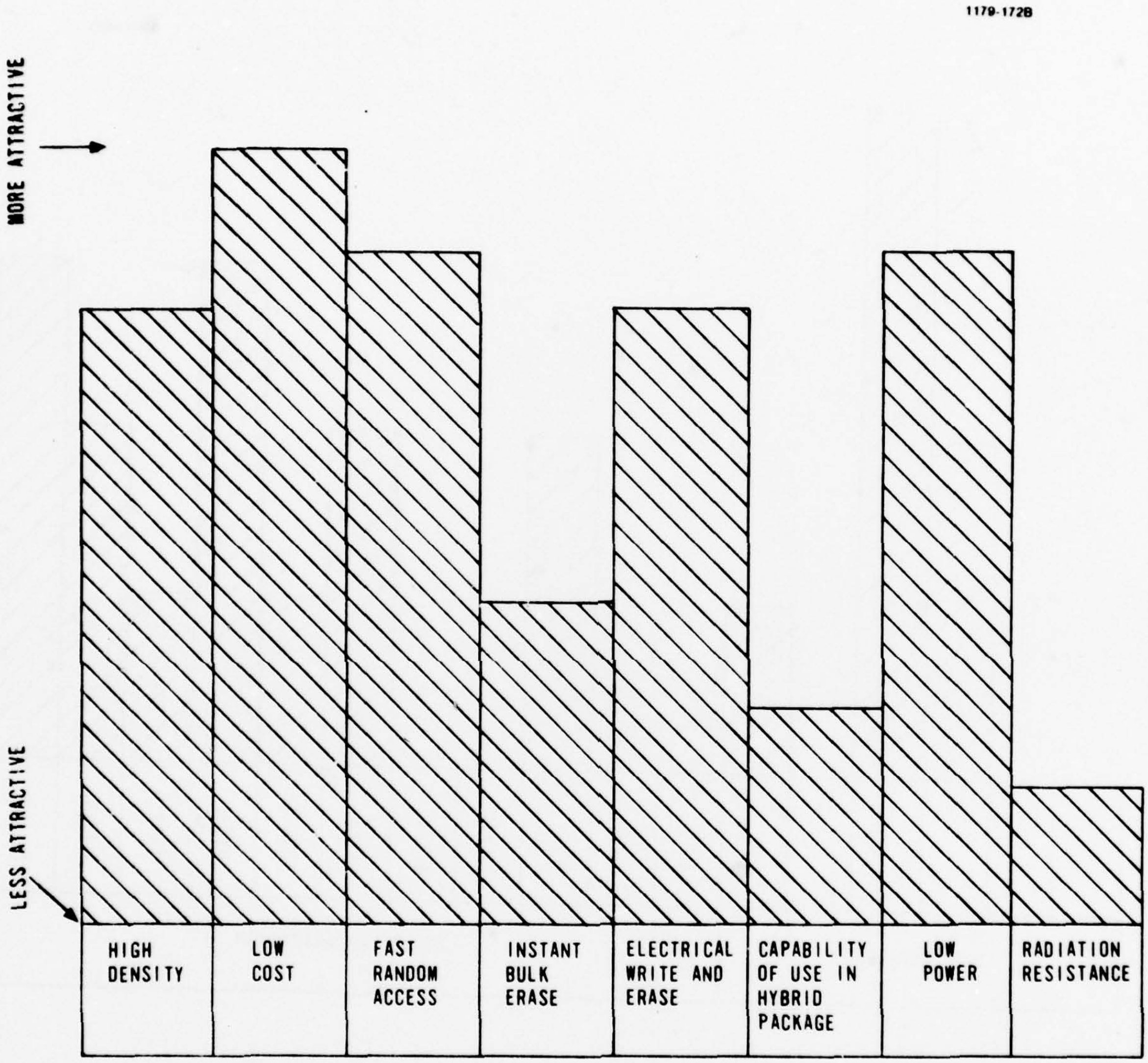


FIGURE 4-2. QUESTION NO. 3
MOST ATTRACTIVE MNOS CHARACTERISTICS

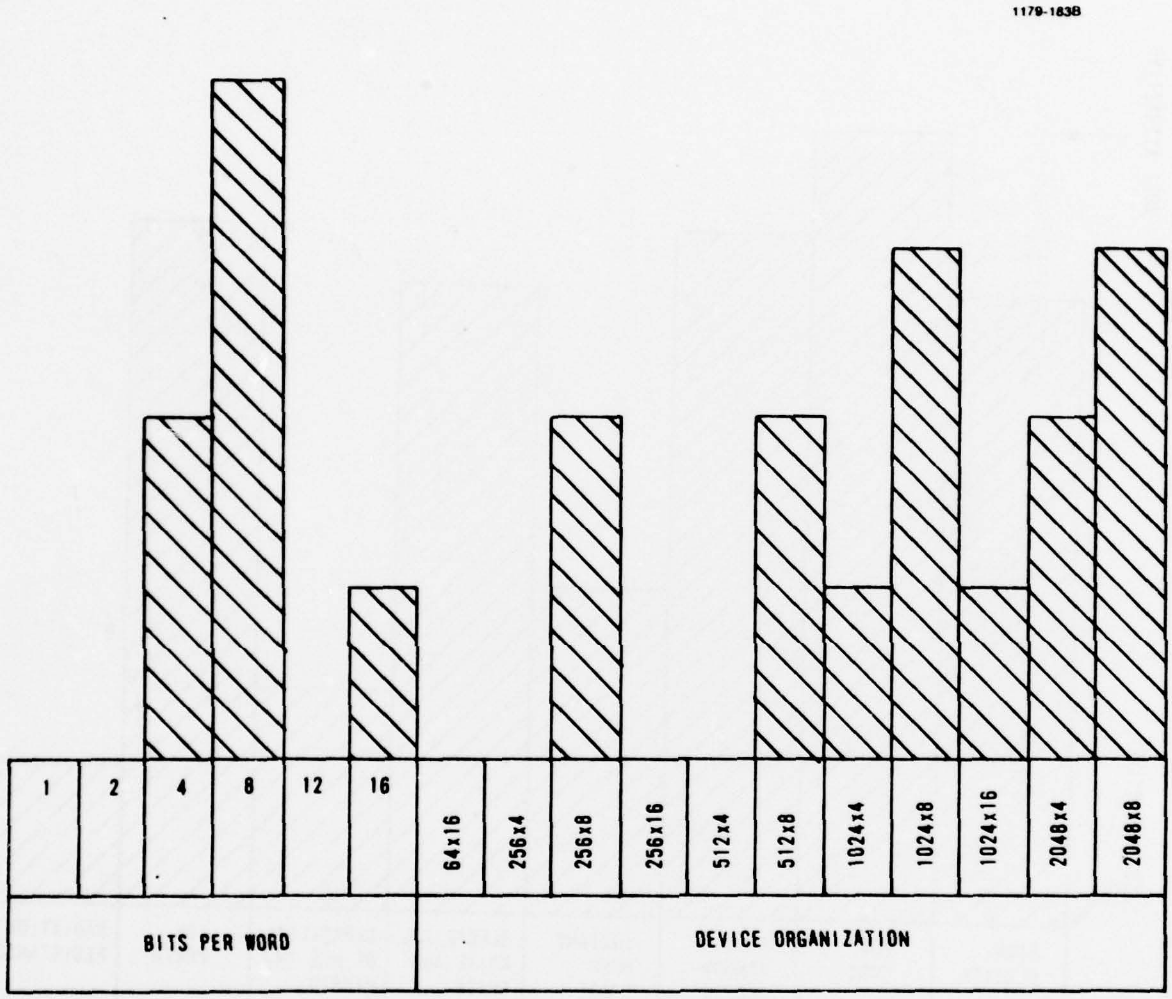
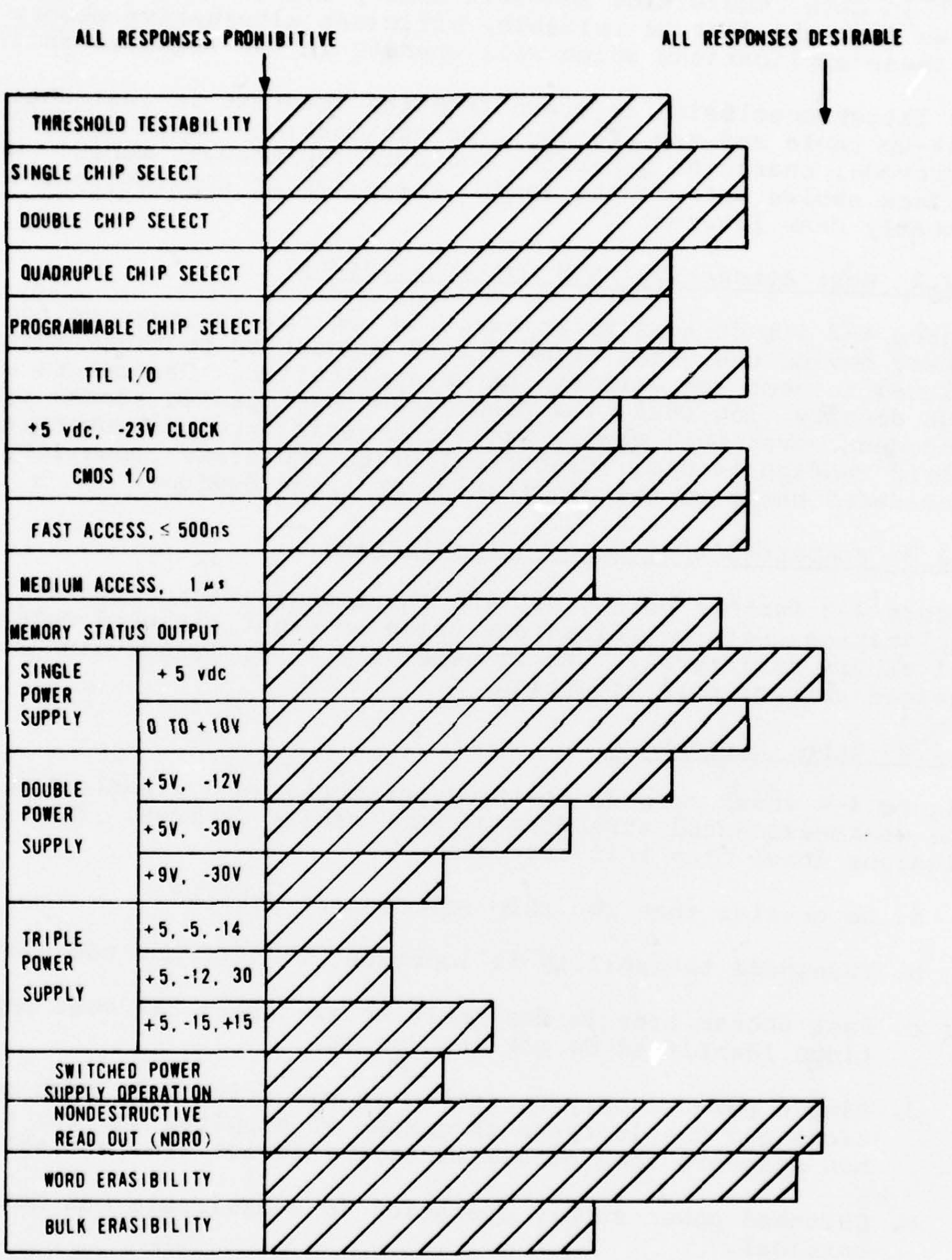


FIGURE 4-3. QUESTION NO. 4
PREFERRED MNOS MEMORY ORGANIZATION



WEIGHTING (P) PROHIBITIVE -0, (U) UNDESIRABLE, BUT NOT PROHIBITIVE -1,
(I) IRRELEVANT TO APPLICATION -2, (C) CRITICALLY IMPORTANT -3,
(S) SIGNIFICANT -4, (d) DESIRABLE -5

FIGURE 4-4. OTHER PARAMETERS

not crucial. The former is shown by the interest in special environment in data acquisition and bulk memory modes. This need probably stems from the lack of reliable, efficient alternative memory types in these applications which will operate in the required environment.

The latter conclusion is drawn from the interest in instruction, look-up table and map storage type applications while ignoring the microcode, character generator and core replacement modes. When MNOS devices evolve into faster speeds these latter applications will probably draw interest.

4.2.2 Most Attractive MNOS Characteristics

Figure 4-2 illustrates to an exacting degree, the reasons for MNOS memory device use. The prime driver appears to be those factors related to cost and versatility of application. Parameters such as high density, low cost, low power and "fast" random access take precedence over bulk erase, radiation resistance and potential use in hybrid configurations. Electrical write and erase capability is considered basic to the application of these devices.

4.2.3 Preferred MNOS Memory Organization

Figure 4-3 further points out the interest in microcomputer type applications with organizations using an eight bit word outstripping all others in interest. As is generally true, larger high density devices attract more attention.

4.2.4 Other Parameters

Figure 4-4 shows more diversified parameters and illustrates some of the weakenesses and strengths of MNOS memory devices. Some conclusions drawn from this data are:

a. No greater than two chip selects are desired.

b. Threshold testability is important to most but not all users.

c. Fast access time is desirable to all users but most applications identified do not require it.

d. Single power supply operation is significant in most applications and the increase in number of supplies and the more non-standard they become makes the device less attractive.

e. Switched power supply operation is undesirable but not critical.

f. Other very desirable features are NDRO, Word Erasability and TTL and/or CMOS compatibility.

g. Bulk erase capability while acceptable for most applications is not as desirable as word erasibility.

4.2.5 Packaging and Temperature Range of Operation

Figure 4-5 illustrates the most desirable packaging schemes and temperature range of operation. From this data it can be seen that the Dual-in-Line (DIP) is significantly more popular than Flat Packs. As was expected the lower the pin count per package, the more popular the package is for military use.

With regard to temperature range of operation a threshold of significant use appears to be -55°C to +85°C. The most significant range of operation was judged to be -55°C to +125°C. This ties in with earlier results which show that special environment is important to MNOS device use in military systems.

4.2.6 Significant Parameters

Figure 4-6 shows the significance of parameters that are specifically related to MNOS device operation such as: retention, endurance and read disturb retention. Cost is included here because of its significance as an initial selection parameter.

a. Time Retention of Data. A threshold for use of these devices appears to be a minimum retention of six months for most applications with a one year minimum retention being the most popular for use.

b. 10^9 reads per memory location before disturbing data is a minimum value for use in most military applications with 10^{12} reads/location minimum being the most desirable requirement.

c. In the important endurance characteristic 10^5 write/erase cycles per memory location is the minimum acceptable for most military use with increasing endurance being more attractive.

d. Regarding cost, 2¢/bit is acceptable for most military use with 0.25¢/bit being the most significant point for wide spread use. As expected decreasing cost/bit is more desirable for device use.

4.2.7 Commercial MNOS Devices

Figure 4-7 shows current use of identified commercially available MNOS device with the NCR/GI 2805 and GI 3400 being most used. While the 2805 is in current use, its replacement by the similar newer device, the 2810, is anticipated in the near future (1979/1980 time frame). The higher density 8K parts (2805/2810) and the faster word organized parts (2451/3400) appear the most popular in current use. The lower density parts of 7050 series of Nitron do not appear popular from these results for military applications.

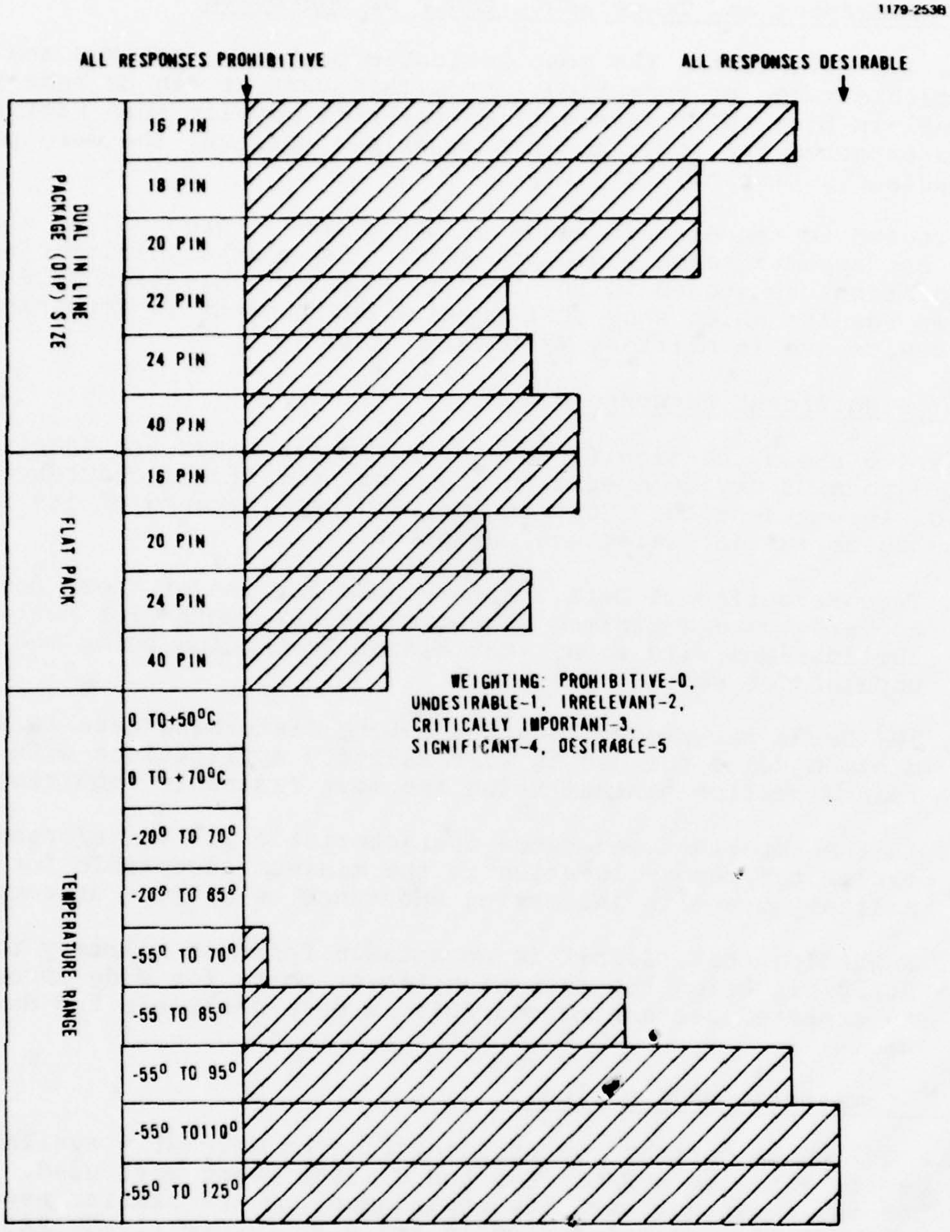


FIGURE 4-5. MOST DESIRABLE PACKAGING AND TEMPERATURE RANGE

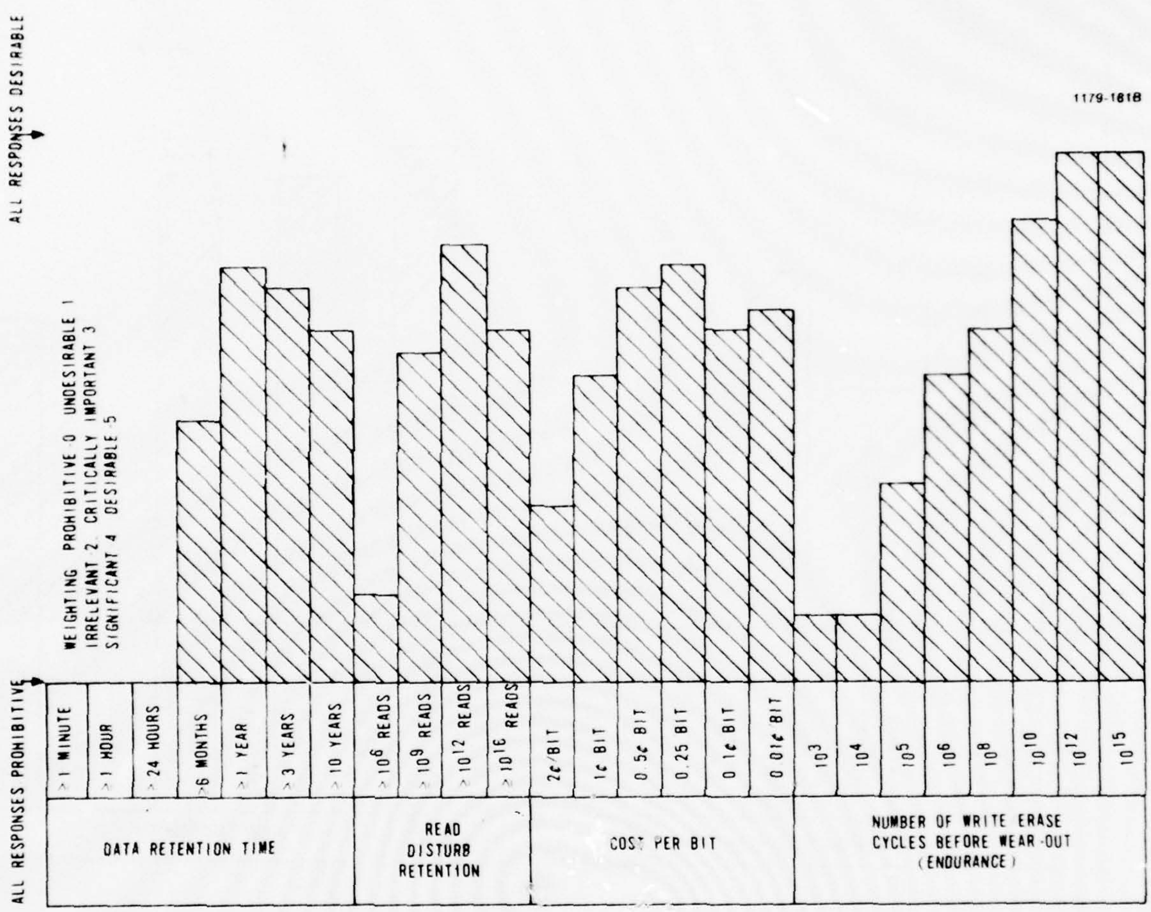


FIGURE 4-6. SIGNIFICANT PARAMETERS

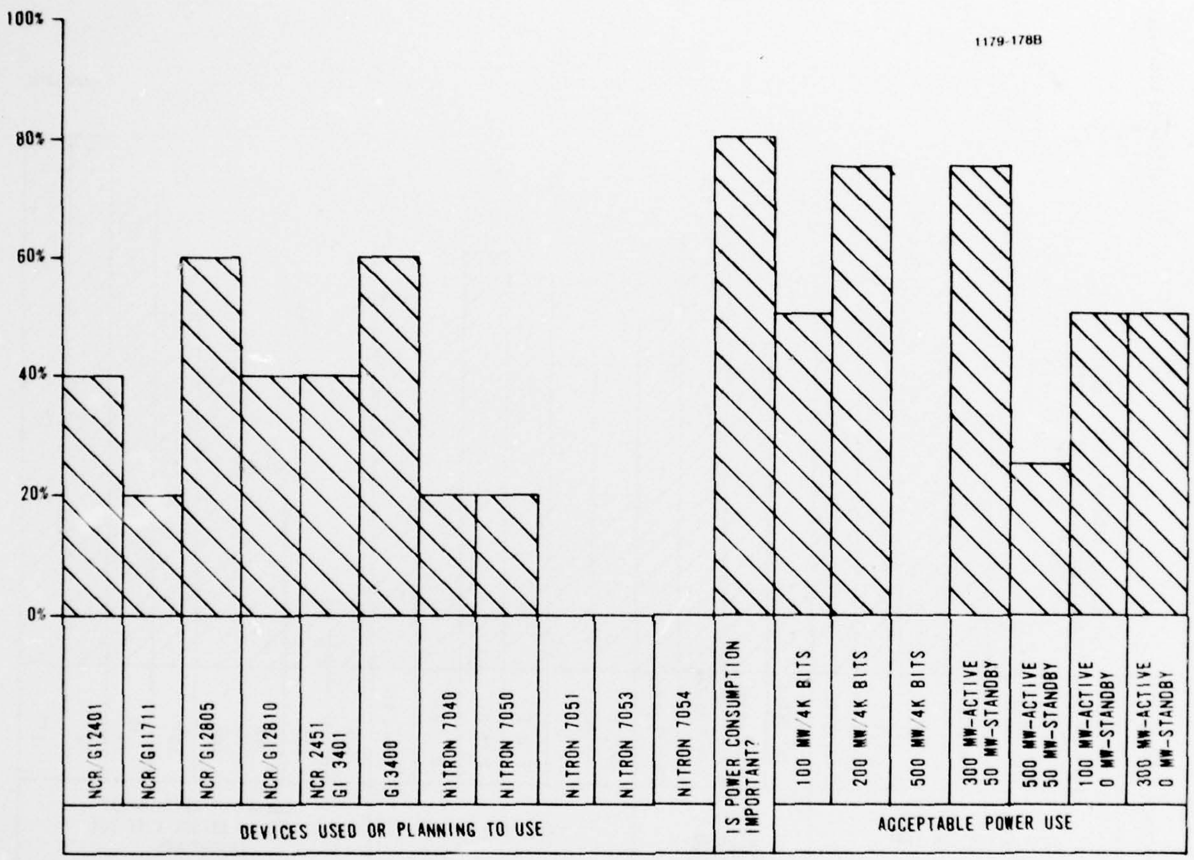


FIGURE 4-7. COMMERCIAL MNOS DEVICES

This figure also illustrates the importance of power dissipation with 80 percent responding that it is significant. The most significant use appears to be in a maximum of 200 mw/4K bits active power or 300 mw/rK bits active and 50 mw standby region.

4.3 MILITARY APPLICATIONS SURVEY SUMMARY AND CONCLUSIONS

In analyzing the results of the Military Applications Survey, several factors not directly apparent should be considered before an accurate picture of an optimum part for near and far term military use can be drawn:

a. Influence of present and past parts on the projection of new applications. This will tend to restrict new designs to tradiational roles.

b. Lack of in-depth understanding of the MNOS technology; its advantages, liabilities and pecularities of proper application; tend to either encourage unrealistic requirements or produce ultra-conservative approaches which reduce its applications capabilities. In some cases this factor may tend to down-play the significance of parameters such as threshold measurment capability and radiation resistance while unrealistically intimidating designers regarding endurance characteristics.

The Applications Survey reflects to a large degree, these characteristics which are significant and desirable in the selection of MNOS devices for military applications. These results must be compared against the actual characteristics of available commercial devices to determine the best fit if any for use in the second phase of the MACI-EAROM program. In some cases the available devices will exceed the desired requirements while in others compromises will have to be made limiting desirable requirements to more practical realizable goals.

The following section on Selection Criteria takes the survey results and molds them with practical goals around which to judge the available parts. This section also integrates the specified requirements of the MACI Program into this criteria development.

Section 5

MNOS MEMORY DEVICE SELECTION CRITERIA

Based on the information gathered from the Military Applications Survey, Honeywell's own experience, and available device information, the Selection Criteria Chart was generated (Table 5-1).

Other criteria not easily shown in chart form are also significant factors in the selection of the most promising device/devices from the available candidates. Some of these are:

a. Memory Transistor Threshold Measurement Capability. While a few respondents felt this capability irrelevant to their application, Honeywell and the majority surveyed felt this to be of critical significance. Without availability of threshold information, retention and endurance prediction and measurement is difficult, inaccurate and questionable. Since these are the most significant factors in the non-volatility of these devices this parameter is considered critical.

b. Mode of Erase. While most respondents felt bulk erasure (i.e., EAROM) of data is less desirable (except in secure systems) it is not considered prohibitive for most applications. Word erase capability is considered desirable or important in most applications.

c. Memory Status Output (i.e., Data Valid Signal). While considered a desirable feature it is secondary in importance to a majority of applications.

d. TTL or CMOS Input/Output Compatibility. Compatibility to TTL input/output levels is considered significant to use in military systems. Compatibility to CMOS I/O levels while desirable is of secondary application significance.

Other factors, which were not sampled by the Applications Survey but are considered significant to use in military systems are:

a. Device manufacturer aspects:

1. Device availability present and future due to:

(a) Production capacity with respect to demand.
(b) Level of vendor priority.
(c) Future support of device.
(d) Yield - difficulty of manufacture.
(e) Multiple sources.

TABLE 5-1. SELECTION CRITERIA

Parameter Classification	Selection Parameter	Optimum Value From Survey	Minimum/Maximum Value for Significant Use	Comments
1. Device Organization	a. Number of bits	16K	2K	8K and 4K bit devices in wide use. MACI Spec ≥-1K bits/device.
	b. Number of Bits/word	8	4	No 8 bit/word devices available (pins/package = lim)
	c. Number of chip selects	2	1	Up to 4 CS is desirable
	d. Programmable chip	1	0	Desirable but unimportant
	e. Number of power supply voltages	1 +5 Vdc	3 +5 Vdc -12V and -30V	Lower no. voltages desirable. Standard voltages important (i.e., +5V, ±15V, ±12V, etc.)
2. Performance characteristics	a. Access Time	500 μs	Undefined	Time access ≤1 μs desirable
	b. Temperature range of operation	-55°C to +125°C	-55°C to +85°C	
	c. Data Retention (Static)	1 yr (10 yrs desirable)	6 mos, 1 yr specified	Some use down to 24 hrs MACI Spec ≥1 yr.
	d. Read Disturb retention (No. of Read Cycles before loss of data)	10^{12} cycles	10^{9} cycles	Some use down to 10^{6} cycles.
	e. Endurance (No. of write/erase cycles before device wearout)	10^{10} E/W cycles/bit	10^{5} E/W cycles/bit	Some use down to 10^{3} cycles. Some systems require 10^{6} E/W cycles.

TABLE 5-1. SELECTION CRITERIA (Continued)

Parameter Classification	Selection Parameter	Optimum Value From Survey	Minimum/Maximum Value for Significant Use	Comments
3. Packaging	a. Package type	Dual-in-ceramic	Flat pack Gold Kovar	Flat pack unacceptable in some MIL Appl
	b. No. pins	16	24	
4. Power Consumption	a. Active Power (no standby)	100 mw/4K bit/dev	200 mw/4K bit dev	NOTE: Power Consumption was considered significant to device use in Military Systems.
	b. Active + stand-by power	100 mw/4K dev Active OW stand-by	300 mw/4K dev Active 50 mw stand-by	
5. Cost	a. Price/Bit	≤0.25¢/bit	≤2.0¢/bit	

2. Level of Quality Control:

    (a) Inspection procedures and relationship to MIL-883-B.
    (b) In process controls.
    (c) Vendor applications support.
    (d) High reliability production line options.

3. Domestic Sources

4. Viability of Manufacturer

b. Current military use. The baseline criteria for device selection are the conditions specified by the MACI program. A listing of these conditions is shown below:

Memory content:	1024 bit minimum
Organization:	256 words x 4 bits (or 1024 wds x 1 bit) minimum
Write/erase Voltages:	±35 volts max.,
Write time:	10 milliseconds max.
Unpowered Data Storage:	3 years min.
Read Access Time:	2 microseconds max.
Endurance:	10^6 E/W cycles min.
Decoding:	Fully decoded column address (Row decoding desired but not necessary)

Initially, a 4K bit max. size was specified but this specification has been removed by joint Honeywell ERADCOM agreement.

Section 6

VENDOR DATA

From the previous section, it can be seen that a large portion of this process is dependent on the status, attitudes and positions taken by candidate device manufacturers (vendors). Since the early days of development of MNOS technology, competing technology advocates have always used device availability arguments due to no or nonviable second-sourcing to push their products instead of MNOS. This report shows the current status of commercially available MNOS device manufacturers with an attempt made to evaluate both the viability of the vendor and his support for candidate devices. An original list of potential vendors proposed were contacted for participating in this program with the following results.

6.1 POTENTIAL DEVICE VENDORS

6.1.1 NCR (National Cash Register), Miamisburg, OH

NCR contacted in July 1978 and exhibited interest in the MACI program. A meeting was set for 5 October 1978.

6.1.2 Nitron Corp., Cuppertino, CA

Nitron was contacted in July 1978 and expressed interest in MACI. A meeting was set for 26 October 1978.

6.1.3 Sperry-Univac, St. Paul, MN

Merton Horne was contacted in July 1978 and visited 27 July 1978. While expressing initial interest in participating upon visiting the facility, a policy decision was made not to make devices available to the commercial market eliminating them from MACI participation.

6.1.4 Westinghouse Corp., Baltimore, MD

Joe Brewer of WH was contacted and confirmed that their devices were not available for commercial use thus eliminating them from MACI participation.

6.1.5 General Instruments Inc., Hicksville, NY

GI was contacted in July 1978 and agreed to participate in the MACI program. A meeting was set for 14 September 1978.

6.1.6 Rockwell International Inc., Anaheim, CA

This company was contacted but stated that no devices were available for MACI (Micheletti).

6.1.7 Actron Corp (MacDonell/Douglas), Huntington Beach, CA

Dr. Vukon Hsia was contacted in July 1978. He stated no EAROM/WAROM type devices were available for MACI and company charter policy was for internal device use only.

6.1.8 Others

Other potential device vendors like RCA, Princeton, NJ and General Electric, Utica, NY, were contacted but have no available devices.

6.1.9 Conclusions

Only three potential device vendors resulted from the initial survey: GI, NCR, and Nitron. While Nitron Corp. makes independently designed devices, all three vendors use the NCR process as a baseline since NITRON and GI were cross licensed to make NCR parts. This results in a majority of candidate devices having current or future multiple sources. The detailed discussions that took place with each potential vendor are shown in Subsections 6.2, 6.3, and 6.4. Subsection 6.5 shows the preseal Quality Inspection procedures for Nitron and NCR and compares them on a point-by-point base with MIL-STD-883-B.

6.2 VENDOR SURVEY REPORT: General Instruments Corporation
Hicksville, New York

Survey Dates

23 February 1979 and 14 September 1978.

Survey Objectives

The first meeting was held to discuss MACI program objectives with GI and determine prospective devices for use in MACI. The second meeting was held to obtain detailed quality inspection plans and discuss some test results and problems with delivery of parts for use in the program.

Results of Meetings

Talks with Michael French (Marketing Manager for MNOS) and Morton Kalet (Engr Manager EAROMS) produced the following results.

a. ER2401 - 1K x 4 EAROM - mature with a lot of test and system data available.

b. ER3400 - 1K x 4 WAROM - mature, flexible part with long term company support.

c. ER2805/2810 - 2K x 4 EAROM - high density, long term support and predicted high volume part.

Further talks mentioned the Non-Volatile RAM approach (i.e., ER1711/1721) as possible alternate parts. Mike French stated that the ER2401 will be phased out in two to three years; the 8K parts (i.e., ER2805/2810) are committed until at least 1983. The ER3400 will have continued support with new N-channel parts to be made compatible. In addition, a low powered version and addition of a memory status output is being considered. A copy of the low power version specification is attached.

GI is doing a lot of commercial MNOS business in TV tuners, particularly in the European market. They plan to develop N-channel MNOS technology as a primary goal. In addition, both P and N channel parts are being developed with on-chip voltage doublers to allow for single voltage operation. A large emphasis will be placed on non-volatile RAM (standard state RAM cell backed up by a MNOS transistor).

GI is willing to sell devices to a high reliability specification to meet military requirements (MIL-883). They also will sell chips and wafers. Devices are available in both ceramic or plastic dual-in-line packages.

The ultimate goal of GI is to build high density N-channel MNOS memory parts. These parts will be for both commercial and military parts.

A Quality Inspection plan was received from GI showing the similarities and differences with GI normal preseal procedures and MIL-STD-883-B. This is shown in Attachment B. A more detailed plan was requested in order to make a point by point comparison with MIL-STD-883, but has not been received. GI states that it is the same as MIL-STD-883-B.

Conclusions

GI will continue to be a stable supplier of MNOS parts in the near term. GI's applications interface needs some attention as misleading, contradictory information is sometimes given for device feedback from users.

From GI comments, the most promising MACI candidates are ER2810/2805 and ER3400/2451. The ER2401 is a lesser candidate due to potential phasing out in the near future.

Facilities

Three plants with total employment of 4,600 people. MNOS development done at Hicksville (900 employees).

Capacity

Two million MNOS parts/year expected in 1979. Total MNOS parts shipped is over three million since start.

6.3 VENDOR SURVEY REPORT: Nitron, Cuppertino, CA

Survey Dates

26 October 1978.

Survey Objective

A trip was made to Nitron to discuss MNOS EAROMs for the MACI Program. It was the objective of this trip to evaluate Nitron's MNOS present and future products as being considered candidates for evaluation for the MACI Program. In addition to candidate discussions, the imposition of MIL-M-38510 and its requirements were also to be discussed.

Results of Meeting

Nitron people contacted: Mr. James Reel, Marketing Manager and
Mr. Wendel Spence, MNOS Process Manager.

Honeywell people in attendance were Mr. R. Novak, Design Support.

On October 26, 1978 Mr. Novak met with Nitron and explained the MACI Program requirements, and in addition, presented the MACI Program Plan. Our plans and objective for the MACI Program were delineated.

Discussions of Nitron's MNOS technology as related to EAROMs was the first item on the agenda. Nitron uses the P-channel MNOS technology and thus far have not utilized an N-channel process. Nitron will second-source the Actron N-channel design once it is established.

Nitron indicated the following EAROMs as possible devices for consideration on this MACI Program:

a. NC7053 - 128 x 8
b. NC7054 - 256 x 4
c. NC2810 - 2K x 4

Nitron indicated that their prime choice of an EAROM for this program would be the NC7053, which is a two transistor-per-bit design. This design is capable of full military temperature operation and is presently undergoing characterization at Nitron. This characterization was to be completed by February 1979. Nitron expressed a willingness to share all their available characterization data with Honeywell.

Nitron will soon receive a new set of corrected mask sets from NCR for the 2810 8K EAROM. Nitron had set their internal priorities such that the 2810 would not become available until April 1979. Nitron will start the 2879 and the 1721 prior to the 2810.

Nitron does about 50 percent military business; most of that is custom circuits. Nitron is building parts for the Parkhill Program (NSA) and have received approval for the requirements of MIL-M-38510, Appendix A. A copy of their preseal visual inspection, as approved by NSA, was obtained. Nitron has a secret facility clearance.

Nitron employs about 100 people at present and are trying to hire more people. It appeared they have a healthy backlog of orders. Nitron has also invested about $400K into a new water purification system. The facility is undergoing changes in order to accommodate their new business. At present, Nitron does no off-shore manufacturing. They have an agreement with Ireland and Israel to construct facilities in these two countries.

Conclusions

Nitron appears to have viable EAROMs, with the added feature of second sources, for possible selection as a candidate for the MACI Program. Nitron appears very willing to work with Honeywell in our endeavor to fulfill the MACI Program requirements. Nitron indicated that they will second-source the NCR 2810 with OEM product becoming available on or about April 1979.

6.4 VENDOR SURVEY REPORT: National Cash Register (NCR) Miamisburg, OH

Survey Date

5 October 1978.

Survey Objective

A trip was made to NCR Microelectronics Division to discuss MNOS EAROMs for the MACI Program. It was the objective of this trip to evaluate NCR's MNOS present and future products as being considered candidates for evaluation for the MACI Program. In addition to candidate discussions, the imposition of MIL-M-38510 and its requirements were also to be discussed.

Results of Meeting

The NCR people contacted were Mr. Larry Hatt, Applications Engineer and Mr. Robert Baugh, QA Manager.

Honeywell people in attendance were Mr. R. Wiker, Engineering and Mr. R. Novak, Design Support.

We explained the MACI Program requirements, and in addition, presented them with the MACI Program Plan. Our plans and objectives for the MACI Program were delineated.

Discussions of the dielectrically isolated MNOS technology as related to EAROMs was the first item on the agenda. The following is a summation of those items discussed.

NCR will phase out the NCR 2401 in two to three years. The operating temperature range of their various devices varied from 70°C to 110°C ambient. NCR felt that the NCR2810 8K EAROM could be characterized to 110°C with very good results. The absolute maximum operating temperature for the 2810 was indicated to be +125°C for very short periods. The MNOS did exhibit a long wait time characteristic between writing and reading at -55°C.

It was indicated that the retention of the MNOS EAROMs shows indication to be governed by the number of erase cycles imposed on the device, while writing does not seem to have any effects on the device. It was quite evident that the nitride thickness was a very important parameter in determining the retention characteristics of EAROMs. The 10-year retention could be specified at +110°C. The MNOS process appears to be temperature sensitive at about +125°C operating ambient with the occurrence of permanent threshold shifts in NCR's opinion.

NCR's dielectrically isolated process appears to have very good characteristics pertaining to radiation hardening aspects. Sandia has written a report on NCR EAROMs.

The Miamisburg, Ohio plant is dedicated to Engineering and Wafer fabrication. Production at present is done in Hong Kong and Mexico, although there are plans to move all production back to the USA. NCR is in the process of building two more plants dedicated to MNOS products. Their long term objective is to have an automated production assembly line.

The subject of NCR available characterization data was discussed with NCR being very willing to supply this data and associated extrapolated curves to Honeywell. They showed a keen interest in working with Honeywell on the MACI Program.

NCR is now in the process of planning to convert their present P-channel MNOS over to a much faster technology which would be the N-channel MNOS. N-channel access times planned are to be in the 400 to 500 nanosecond range. N-channel technology will not be viable in the time frame for the MACI Program. N-channel technology will provide for higher density circuits with a goal of 5 volt operation.

At present NCR has no OEM business, although they expect this to change in the near future to around 15 to 20 percent. NCR now has cross-license agreements with Nitron, General Instrument and will shortly announce a large Silicon Vally Semi house as another cross-license.

A tour of the facility was made in which all modern, up-to-date machines were in use. Their system operation was compared to the requirements of MIL-M-38510 and it was evident that they parallel 38510 very closely. Wafer fab is being done in 3.0-inch wafers, their largest MNOS chip size being 0.280 x 0.280, with an employee count of around 250 people at Miamisburg. The facility layout and modus operandi appeared quite acceptable. NCR showed a willingness to perform MIL-STD-883 preseal visual to test condition B with a few exceptions; these exceptions are forthcoming.

Conclusions

NCR appears to have viable EAROMs, with the added feature of second sources, for possible selection as a candidate for a EAROM for the MACI Program. NCR appears aggressive and very willing to work with Honeywell in our endeavor to fulfill the MACI Program requirements.

NCR recommends use of NCR2810 and NCR2451 devices for the MACI Program.

Facilities

MNOS is made at Miamisburg, OH plant only. The total employment at Miamisburg is 350.

Capacity

Miamisburg ships 3.0 million ICs per year, of which 2.4 million are MNOS.

6.5 PRESEAL INSPECTION CRITERIA

Objective

To compare the various vendor's preseal inspection criteria with MIL-STD-883B Internal Visual Inspection Method 2010.3 and note dissimilarities which are applicable to MNOS EAROM processes.

Procedure

Preseal visual inspection procedures from Nitron and National Cash Register (NCR) were compared in tabular form to MIL-STD-883B Method 2010.3 (see Tables 6-1 and 6-2). Preseal visual inspection procedures from General Instrument (GI) were not included in the comparisons due to lack of cooperation from the vendor in acquiring the necessary in-house documents.

To use Tables 6-1 and 6-2, trace horizontally across the page from the MIL-STD-883B paragraph to the corresponding paragraph in the vendor column. A blank in the vendor column designates no vendor criteria corresponding to the particular paragraph of MIL-STD-883B. Comments in the last column highlight vendor criteria which differs from MIL-STD-883B or paragraphs of MIL-STD-883B which do not apply to MNOS devices. Note, however, that no comments are made where no equivalent vendor criteria exists to compare to MIL-STD-883B or where vendor criteria is equivalent to MIL-STD-883B.

Results

Comparing each paragraph of MIL-STD-883B Method 2010.3 procedure with each vendor's internal inspection procedure, the following results were obtained:

a. Nitron. There are seven paragraphs in which the criteria does not meet the respective MIL-STD-883B criteria and twenty three MIL-STD-883B paragraphs for which there is no corresponding Nitron paragraph.

b. NCR. There are seven paragraphs in which the criteria does not meet the respective MIL-STD-883B criteria and thirty seven MIL-STD-883B paragraphs for which there is no corresponding NCR paragraph.

c. GI. No comparison was made due to lack of data. Document included indicates MIL-883B relationship but no detailed plan is available.

6.5.1 National Cash Register

Table 6-1 compares MIL-STD-883B requirements with those of NCR visual inspection criteria.

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
1. PURPOSE. The purpose of this test is to check the internal materials, construction, and workmanship of microcircuits for compliance with the requirements of the applicable procurement document. This test will normally be used prior to capping or encapsulation on a on a 100 percent inspection basis to detect and eliminate devices with internal defects, that could lead to device failure in normal application. It may also be employed on a sampling basis prior to capping to determine the effectiveness of the manufacturer's quality control and handling procedures for microelectronic devices. Complex microcircuits may require substitution of alternate screening procedures for visual inspection criterion pertaining to metal coverage, oxide, and diffusion faults that are difficult or impractical to perform. These alternate screening methods and procedures are documented in Method 5004, and their use shall be on an optional basis. Test condition A provides a rigorous and detailed procedure for internal visual inspection intended for high reliability class S microcircuits. Test condition B provides procedures for internal visual inspection intended for classes B and C microcircuits (classes of microcircuits refer to screening requirements of Method 5004).	1. PURPOSE. The purpose of inspection is to check the internal construction, materials and workmanship of Monolithic P-channel MOS integrated circuits and eliminate those devices with internal defects which could lead to device failures in normal operation.	
2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification(s) and any visual standards (gages, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixturing shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.	2. APPARATUS. The apparatus for this test shall include equipment capable of the specified magnification and any visual standards (gages, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixturing for handling devices during examination to promote efficient operation without damaging the units shall be provided. Equipment required shall include at least the following: Microscope (vertical illumination) - Nikon, Olympus N or equivalent. Vacuum Pickup Pencil with Teflon Tip Finger cots for preseal inspection	

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
3. PROCEDURE a. General. The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the requirements of the applicable procurement document and the criteria of the specified test condition. For nonJAN devices if a specified visual inspection requirement is in conflict with circuit design topology or construction, it shall be documented and and specifically approved by the procuring activity. For JAN devices there shall be no waivers. The inspections and criteria in this method shall be required inspections for all devices and locations to which they are applicable. Where the criterion is intended for a specific device process or technology, it has been indicated. b. Sequence of Inspection. The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Visual criteria specified in 3.1.1.2, 3.1.1.5, 3.1.1.7, 3.1.2, 3.1.7 e and f, 3.1.9 a through d, and 3.2.1.2, 3.2.1.5, 3.2.1.7, 3.2.2, 3.2.7 e and f, 3.2.8, 3.2.9 a, b, and d may be examined prior to die attachment without required reexamination after die attachment. Visual criteria specified in 3.1.6.2, 3.1.6.3, 3.2.6.2 and 3.2.6.3 may be examined prior to bonding without reexamination after bonding. Visual criteria specified in 3.2.1.1 and 3.2.3 may be examined prior to die attachment at "high magnification" provided they are reexamined after die attachment at "low magnification". When inverted mounting techniques are employed, the inspection criteria contained herein that cannot be performed after mounting shall be conducted prior to attachment of the die. c. Inspection Control. In all cases, examination prior to final preseal inspection shall be performed under the same quality program that is required at the final preseal inspection station. Care shall be exercised after inspections per 3 b, to insure that defects created during subsequent handling will be detected and rejected at final preseal inspection. During the time interval between visual inspection and preparation for sealing devices shall be stored in a controlled environment. Devices examined to 3.1.	3. PROCEDURE The device shall be examined in a suitable sequence of observations and at the specificied magnification to determine compliance with the requirements of this specition. "High magnification" inspection shall be performed perpendicular to the die surface with the device under illumination normal to the die surface. "Low magnification" inspection shall be performed with either a monocular, binocular or stereo microscope and the inspection performed within an angle of 30 degrees from the perpendicular to the die surface with the device under suitable illumination. Proper control shall be exercised after wafer or slice inspections to insure that defects created during handling will be detected and rejected at final preseal inspection. All references herein to silicon oxide or oxide shall also apply to any other passivation or underlying material used in fabrication monolithic, multichip, or hybrid microcircuits. Wherever the criteria of "0.1 mil of oxide or metal" is used, a "line of oxide" or "line of metal" may be substituted, if, at the magnification at which the inspection is performed, at least 0.1 mil is required to provide a recognizable line of oxide or metal. Where product acceptance is based on reinspection, such reinspection shall be accomplished at the minimum levels specified herein or, where a level higher than the minimum has been specified, reinspection shall be at that specified level.	Procedure instructions are directly comparable, as is inspection criteria, and therefore is included for individual comparison.
3.2 Test Condition B. Internal visual examination as required in 3.2.1 through 3.2.6 shall be conducted on each microcircuit and each integrated circuit chip. In addition, the applicable criteria in 3.2.7 through 3.2.9 shall be used for the appropriate microcircuits areas where glassivation, dielectric isolation or	3.1 Die Inspection. Dice in carriers will be inspected on a 100 percent basis by the inspectors. Normal magnification will be 100X. A higher magnification may be used if necessary to determine a decision.	

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
film resistors are used. The "high magnification" inspection shall be performed within the range of 75X to 150X and the "low magnification" within the range of 30X to 60X.		
3.2.1 Metallization Defects "High Magnification". No device shall be acceptable that exhibits the following in the operating metallization.	3.1.2 Metallization Defect (100X). No device shall be acceptable which exhibits the following in the operating circuit metallization:	
3.2.1.1 Metallization Scratches. A scratch in any tearing defect, including probe marks. in the surface of the metallization.	3.1.2.1 Metallization Scratches. A scratch is defined as any tearing defect that disturbs the original surface of the metallization.	
a. Scratch in the metallization excluding bonding pads, that exposes underlying passivation anywhere along its length and leaves less than 50 percent of the original metal width undisturbed (see Figure 2010-16).	a. A scratch in the metallization that exposes oxide anywhere along its length and leaves less than 50 percent of the original metal remaining (see Figure 2).	
b. Scratch that completely crosses a metallization path and damages the surface of the surrounding passivation on both sides. (For MOS devices, the path shall be the (L) dimension (see Figure 2010-18).)		
c. Scratch in multilayered metallization that exposes the underlying metal anywhere along its length and leaves less than 25 percent of the top-layer original metal width undisturbed (see Figure 2010-16).		
NOTE: Criteria of 3.2.1.1 a, b, and c can be excluded for peripheral power or ground metallization where parallel paths exist such that an open at the scratch would not cause an unintended isolation of the metallization path. When application of this exclusion causes or permits a device design to exceed the current density limitation imposed by the procurement document, this exclusion shall not apply. Current density shall be determined by design not visual inspection.		
d. Scratch in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.	b. Any scratch in the metallization over an oxide step which leaves less than 50 percent of the original metal width remaining.	Vendor's criteria does not meet 883B criteria.
NOTE: Criteria of 3.2.1.1 a through d can be excluded for the last 25 percent of linear length of the contact cut and all metal beyond on the termination end(s) of the metallization runs. In these cases there shall be at least 50 percent of the contact opening area covered by metallization and at least a continuous 40 percent of the contact opening perimeter covered by undisturbed metallization (see Figure 2010-17).		

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
c. Void(s) in the metallization over the gate oxide bridge that leaves less than 75 percent of the metallization length (l) between source and drain diffusions undisturbed (see Figure 2010-18) (applicable to MOS structures).		
d. Void(s) that leave less than 60 percent of the metallization area over the gate oxide bridge undisturbed (applicable to MOS structures).		
e. Void(s) that leaves less than 75 percent of the metallization width coincident with the source or drain diffusion junction line, undisturbed (see Figure 2010-18) (applicable to MOS structures).		
f. Void(s) in the bonding pad area that leaves less than 75 percent of its original unglassivated metallization area undisturbed.		
g. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width (see Figure 2010-20).		
NOTE: If two or more stripes enter a bonding pad, each shall be considered separately.		
h. Void(s) in the metallization of a thin film capacitor that reduces the metallization area by more than 25 percent.		
3.2.1.3 <u>Metallization Corrosion</u>. Any metallization corrosion.	3.1.2.3 <u>Metallization Corrosion</u>. Evidence of metallization corrosion.	
3.2.1.4 <u>Metallization Adherence</u>. Any metallization lifting, peeling, or blistering.	3.1.2.4 <u>Metallization Adherence</u>. Evidence of metallization lifting, peeling, or blistering.	
3.2.1.5 <u>Metallization Probing</u>. Criteria contained in 3.2.1.1 shall apply as limitations on probing damage.	3.1.2.5 <u>Metallization Probing</u> 3.1.2.5.1 Non-wire bond pad areas. Scratch and void criteria (see 3.1.2.1 and 3.1.2.2) shall apply as limitations on probing damage. 3.1.2.5.2 Wire bond pad areas. 3.1.2.5.2.1 Probing damage which leaves less than 75 percent of the remaining pad metallization,	See scratch and void criteria.
3.2.1.6 <u>Metallization Bridging</u>. Any metallization bridging where the separation between any two metallization paths is reduced to less than 0.1 mil, unless by design.	3.1.2.6 <u>Metallization Bridging</u>. Bridged metallization defects that reduce the distance between any two metallization strips to less than 0.1 mil separation whether caused by smears,	

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
	photolithographic defects, or other defects. (NOTE: Do not reject for alloy triangles. Alloy triangles have the appearance of triangular metallic areas which in certain instances may appear to bridge metallization strips.)	
3.2.1.7 Metallization Alignment.	3.1.2.7 Metallization Alignment.	
a. Contact window that has less than 50 percent of its area covered by metallization.	a. Any contact window that has less than 25 percent of its area covered by the metallization.	Vendor's criteria does not meet 883B criteria.
b. Contact window that has less than 40 percent of its perimeter covered by metallization. NOTE: When, by design, metal is completely contained in a contact window, criteria 3.2.1.7 b perimeter coverage can be deleted.		
c. A metallization path not intended to cover a contact window that is separated from the window by less than 0.1 mil.	b. A metallization path not intended to cover a contact window which is separated from the window by less than 0.1 mil.	
d. Any exposure of the gate oxide bridge from source to drain diffusions (see Figure 2010-21) (applicable to MOS structures).		
e. Any exposure of the gate oxide bridge that leaves less than 75 percent of the metallization coincident with the source and drain diffusion junction line undisturbed (applicable to MOS structures).		
f. Gate metallization not coincident with or extending over the diffused guard ring. NOTE: Criteria 3.2.1.7 f applies to MOS structures containing a diffused guard ring. MOS devices that do not contain a diffused guard ring shall have gate metallization extending not less than 0.1 mil beyond the gate oxide bridge (see Figures 2010-18 and 2010-21).		
3.2.2 Diffusion and Passivation Layer(s) Faults, "High Magnification". No device shall be acceptable that exhibits the following:	3.1.3 Oxide and Diffusion Faults (100X). No device shall be acceptable which appears to exhibit any oxide defect under metallization or polysilicon bridging two diffusions (see Figure 4).	Vendor's criteria does not meet 883B criteria.
a. A diffusion junction line that unintentionally crosses another diffusion junction line (see Figure 2010-22).		
b. Any isolation diffusion that is discontinuous except isolation walls around unused areas or bonding pads or any other diffused area with less than 25 percent of the original diffusion width remaining.		

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
c. Either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallization (see Figure 2010-25). NOTE: Double or triple lines indicate that it can have sufficient depth to penetrate down to bare silicon; however, should the absence of glassivation in the defect area or the characteristics of the glassivation present allow verification of the presence or absence of passivation by color or color comparisons, respectively, then these techniques may be used.		
d. An active junction not covered by passivation, unless by design.		
3.2.3 Scribing and Die Defects, "High Magnification." No device shall be acceptable that exhibits:	3.1.1 Scribing Defects (100X). No device shall be acceptable which appears to exhibit the following:	
a. Less than 0.1 mil of passivation visible between operating metallization or bond periphery and edge of the die. NOTE: Criteria of 3.2.3 a can be excluded for beam leads and peripheral metallization including bonding pads where the metallization is at the same potential as the die.	a. Less than 0.1 mil of oxide visible between active metallization and/or bond periphery and edge of the die. Excluded from these criteria are peripheral ground metallization, inactive metallized scribe lines, and bonding pads grounded to the die.	
b. A chipout in the active circuit area (see Figures 2010-24 and 2010-25). NOTE: Criteria 3.2.3 b can be excluded for peripheral metallization that is at the same potential as the die. In these cases there shall be at least 50 percent of the peripheral metallization width undisturbed at the chipout.	b. Any chipout or crack in the active circuit area (see Figure 1).	
c. Any substrate or passivation crack in the active circuit area or a crack that exceeds 5.0 mils in length (see Figure 2010-24).	c. Any crack which exceeds 4.0 mils in length or comes closer than 0.1 mil to any active metallization, bonding pad, or other active portion of the die (see Figure 1).	
d. Any crack that comes closer than 0.1 mil to any operating metallization or other active circuit area on the die (see Figure 2010-24). NOTE: Criteria of 3.2.3 d can be excluded for peripheral metallization that is at the same potential as the die.		
e. A crack, that exceeds 1.0 mil in length, inside the scribe grid or scribe line that points toward operating metallization or functional circuit elements (see Figure 2010-24).	d. Any crack that exceeds 1.0 mil in length inside the scribe line that points toward active metallization or circuit area (see Figure 1).	

1079-16060

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
f. Exposed silicon extending beyond the passivation edge at the point of the beam lead exit from the die (see Figure 2010-25) (applicable to beam lead structure).		Not applicable to this device.
g. A crack that comes closer than 0.5 mil to operating beam lead metallization (see Figure 2010-25).		
	e. Any latent chipouts greater than 4 mils in length (4 mils is equivalent to the narrow dimension of a bonding pad).	
	f. On 4 phase custom arrays only, two or more chipouts which reduce the p region conductive path to less than 50 percent in the area adjacent to a bonding pad.	
	3.2 Preseal Inspection (Wire Bond Inspection)	
	Preseal inspection will be performed on a 100% basis by the inspectors. Normal magnification will be 50 to 100X. During the time interval between preseal inspection and package sealing, devices shall be stored in a dry, dust-free, positive pressure, inert controlled environment.	Vendor's criteria 3.2.1 through 3.2.3 is the same as or less than vendor criteria 3.1.1 through 3.1.3.
	3.2.1 <u>Scribing and Die Defects (100X)</u>. No device shall be acceptable which appears to exhibit the following:	
	a. Less than 0.1 mil of oxide visible between active metallization and/or bond periphery and edge of the die. Excluded from these criteria are peripheral ground metallization, inactive metallized scribe lines, and bonding pads grounded to the die.	
	b. Any chipout or crack in the active circuit area (see Figure 1).	
	c. Any crack which exceed 4.0 mils in length or comes closer than 0.1 mil to any active metallization, bonding pad, or other active portion of the die (see Figure 1).	

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
	3.2.2 Metallization Defects (100X). No device shall be acceptable which exhibits the following in the operating circuit metallization.	
	3.2.2.1 Metallization Scratches. A scratch is defined as any tearing defect that disturbs the original surface of the metallization.	
	a. A scratch in the metallization that exposes oxide anywhere along its length and leaves less than 50 percent of the original metal width undisturbed (see Figure 3).	
	b. Any scratch in the metallization over an oxide step which leaves less than 50 percent of the original metal width undisturbed.	
	3.2.2.2 Metallization Voids. A void is defined as any region in the metallization where oxide is visible that is not caused by a scratch.	
	a. A void in the metallization which leaves less than 50 percent of the remaining metal width undisturbed (see Figure 3).	
	b. Any void in the metallization over an oxide step which leaves less than 50 percent of the remaining metal undisturbed.	
	3.2.2.3 Metallization Corrosion. Evidence of metallization corrosion.	
	3.2.2.4 Metallization Adherence. Evidence of metallization lifting, peeling, or blistering.	
	3.2.2.5 Metallization Probing. Scratch and void criteria (see 3.2.2.1 and 3.2.2.2) shall apply as limitations on probing damage.	

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
	3.2.2.6 Metallization Bridging. Bridged metallization defects that reduce the distance between any two metallization stripes to less than 0.1 mil separation whether caused by smears, photolithographic defects, or other defects. (NOTE: Do not reject for alloy triangles. Alloy triangles have the appearance of triangular metallic areas which in certain instances may appear to bridge metallization stripes).	
	3.2.2.7 Metallization Alignment.	
	a. Any contact window that has less than 25 percent of its area covered by the metallization.	
	b. A metallization path not intended to cover a contact window which is separated from the window by less than 0.1 mil.	
	3.2.3 Oxide and Diffusion Faults (100X). No device shall be acceptable which appears to exhibit any oxide defect under metallization or polysilicon bridging two diffusions (see Figure 4).	
3.2.4 Bond Inspection, "Low Magnification". This inspection and criteria shall be required inspection for the bond type(s) and location(s) to which they are applicable when viewed from above. NOTE: Wire tail is not considered part of the bond when determining physical bond dimensions.	3.2.4 Bond Inspection (30X to 50X). The inspection and criteria in this paragraph shall be required inspection for the bond type(s) and location(s) to which they are applicable.	
3.2.4.1 Gold Ball Bonds. No device shall be acceptable that exhibits:	3.2.4.2 Gold Ball Bonds. No device shall be accepted that exhibits:	Vendor's criteria exceeds 883B.
a. Gold ball bonds on the die or package post where the ball bond diameter is less than 2.0 times or greater than 6.0 times the wire diameter.	a. Gold ball bonds on the die or package post where the ball bond is less than two times or greater than five times the wire diameter.	
b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.	b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.	
c. Gold ball bonds where the wire center is not within the boundaries of the bonding pad.	c. Gold ball bonds where the wire exit is not completely within the periphery of the ball.	

1079-16060

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
d. Intermetallic formation extending radially more than 0.1 mil completely around the periphery of any gold ball bond for that portion of the gold ball bond located on metal.	d. Intermetallic formations extending radially more than 0.1 mil completely around the periphery of any gold ball bond located on metal.	
	e. Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding pad area.	
	f. Neck down of bond wire less than 50 percent diameter.	
3.2.4.2 <u>Wedge Bonds</u>. No device shall be acceptable that exhibits:	3.2.4.1 <u>Wedge Bonds</u>. No device shall be acceptable acceptable which exhibits:	Vendor's criteria exceeds 883B.
a. Ultrasonic wedge bonds on the die or package post that are less than 1.2 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 5.0 times the wire diameter in length (see Figure 2010-26).	a. Wedge bonds on the silicon die or package post that are less than 1.2 times or more than 2.5 times the wire diameter in width or which are less than 1.5 or more than 3.5 times the wire diameter in length.	
b. Thermocompression wedge bonds on the die or package post that are less than 1.5 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 5.0 times the wire diameter in length (see Figure 2010-26).		
c. Wedge bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe (see Figures 2010-20 and 2010-27).		
NOTES: 1. Criteria 3.2.4.2 c can be excluded when the entering metallization strip is greater than 2.0 mils in width and the bond pad dimension on the entering metal stripe side is greater than 3.5 mils. 2. The requirements of 3.2.4.2 c for a visual line of metal can be satisfied when an acceptable wire tail obscures the area of concern, providing the following condition exists: Bond is located more than 0.1 mil from the intersecting line of the entering metallization stripe and the bonding pad, and there is no visual evidence of disturbed pad metallization at the bond and wire tail interface.		

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
	b. Wedge bonds where less than 50 percent of the bond is within the unpassivated bonding pad area.	
3.2.4.3 <u>Tailless Bonds (Crescent)</u>. No device shall be acceptable that exhibits:		
a. Tailless bonds on the die or package post that are less than 1.2 times greater than 5.0 times the wire diameter in width, or are less than 0.5 times or greater than 3.0 times the wire diameter in length (see Figure 2010-26).		
b. Tailless bonds where the bond impression does not cover entire width of the wire.		
c. Tailless bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undistributed metal visible between the periphery of the bond and at least one side of the entering metallization stripe (see Figure 2010-27).		
3.2.4.4 <u>General (Gold Ball, Wedge, and Tailless)</u>. No device shall be acceptable that exhibits:	3.2.4.3 <u>Bonding - General</u>	
a. Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding pad area.		
b. Bonds on the package post that are not completely within the boundaries of the package post.	g. Package "post" bonds which are not *completely within the* edge of the "post" pattern.	
	a. Rebonding shall be limited to 10 percent of the total number of bonds.	
	b. Rebonding individual pad locations shall be limited to one rebond attempt.	
	c. Bonding direction shall be pad to post unless Engineering AUTHORIZES deviation for Product Code.	
	No device shall be acceptable which exhibits:	
c. Bonds placed so that the wire exiting from the bond crosses over another bond.	a. Bonds placed so that the wire exiting from the bond crosses	

1079-16060

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
	over (when viewed from above) or appears to contact another unpassivated wire or bond (except the ground wire and its die wire).	
d. Bonds placed so that the separation between bonds or the bond and operating metallization not connected to it is less than 0.1 mil.	e. Bonds placed so that the separation between bonds or the bond and adjacent metallization not connected to it is less than 0.1 mil.	
e. Wire bond tails that extend over or make contact with any metallization not covered by glassivation and not connected to the wire.	f. Wire tails which extend over (when viewed from above) or make contact with any metallization not covered by passivation and not associated with the wire. In addition, any wire tails which exceed two wire diameters in length at the pad and four wire diameters at the post.	
f. Wire bond tails that exceed two wire diameters in length at the bonding pad or four wire diameters in length at the package post.		
g. Bonds where less than 50 percent of the bond is located within an area that is free of die preform mounting material.		
h. A bond on top of another bond, bond wire tail or residual segment of lead wire. An ultrasonic wedge bond alongside a previous bond where the observable width of the first bond is reduced less than 0.25 mil, is considered acceptable.		
i. Any evidence of repair of conductors by bridging with or addition of bonding wire or ribbon.		
j. Any rebonding which violates the applicable rework limitations of MIL-M-38510.		
	h. A wire which crosses another bonded post pad.	
	i. A wire bond which has damaged the passivation layer (silox) and leaves a residue of continuous metallic particles on the silox such as to caude bridging.	
	j. Wire loop height shall not be higher than 0.015 inch nor less than 0.005 inch above the package post surface area.	
	k. Bonds which are attached to preform wetting area should be avoided where possible.	

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
3.2.4.5 **Beam Lead**. This inspection and criteria shall apply to the completed bond area made using either direct tool contact or a compliant intermediate layer. No device shall be acceptable that exhibits. a. Bonds where the tool impression does not completely cross the entire beam width. b. Bonds on thin film substrate metal where the tool impression increases the beam lead width less than 15 percent (10 percent for compliant bonds) or greater than 75 percent of the undeformed beam width. c. Bonds where the tool impression length is less than 1.0 mil (see Figure 2010-28). d. A bonding tool impression less than 1.0 mil from the die edge (see Figure 2010-29). e. Effective bonded area less than 50 percent of that which would be possible for an exactly aligned beam (see Figure 2010-28). f. Cracks or tears in the effective bonded area of the beam greater than 50 percent of the original beam width. g. Bonds placed so that the separation between bonds or between bonds and operating metallization not connected to them is less than 0.1 mil. h. Bonds lifting or peeling.		Not applicable to this device.
3.2.5 Internal Leads, "Low Magnification". This inspection and criteria shall be required inspection for the lead type(s) and location(s) to which they are applicable.	3.2.5 Internal Lead Wires (30X to 50X). No device shall be acceptable which exhibits:	
3.2.5.1 Wires. No device shall be acceptable that exhibits: a. Any wire that touches another wire (excluding common wires), package post, unglassivated operating metallization, die, or any portion of the package.	a. Excessive loop or sag in any wire such that it could short to another unpassivated wire, pad, package, post, die or touch any portion of the package.	
b. Excessive loop or sag in any wire so that it comes closer than two wire diameters to another wire, package post, unglassivated operating metallization or die, or portion of the package after a spherical radial distance from the bond perimeter on the die surface of 5.0 mils for ball bonds, or 10 mils for ultrasonic and thermocompression bonds.	e. Wires which are separated by less than three wire diameters at a distance of 10 mils above the die surface.	Vendor's criteria does not meet 883B criteria.
c. Nicks, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent.	b. Nicks, cuts, crimps, scoring, or neckdown of the bonding wire which reduce the wire diameter by more than 25 percent. c. Missing lead wires or attached extra lead wires greater than two wire diameters in length at the pad or four wire diameters in length at the post.	

1079-16060

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
d. Attached extra wire greater than two wire diameters in length at the bonding pad or four wire diameters in length at the package post.		
e. Tearing at the junction of the wire and bond.	d. Tearing at the junction of the wire and bond.	
f. Any wire making a straight line run from die bonding pad to package post that has no arc.		
g. Wire(s) crossing wire(s) (except common conductors).		
h. Wire(s) not in accordince with bonding diagram.		
3.2.5.2 Beams. No device shall be acceptable that exhibits the following between the edge of the die and the bond area:		Not applicable to this device.
a. Voids, nicks, depressions, or scratches that leave less than 50 percent of the beam width undisturbed.		
b. Beam separation from the die.		
c. Missing or partially fabricated beam leads, unless by design.		
d. Beam leads that are not bonded.		
e. Bonded area closer than 0.1 mil to the edge of the passivation layer.		
f. Lack of evidence of a passivation layer between the die and each beam (see Figure 2010-25 and 2010-28).		
3.2.6 Package Conditions, "Low Magnification". No device shall be acceptable that exhibits:		
3.2.6.1 Foreign Material. All foreign material or particles may be blown off with a nominal gas blow (approximately 20 psig). The device shall then be inspected and be rejected when it exhibits the following:	3.2.6 Foreign Material (30X to 50X). No device will be acceptable which exhibits: f. General: Material shall be considered attached when it cannot be removed by a nominal gas blow (approximately 20 psig). Conductive foreign material is defined as any substance which appears opaque under all conditions of lighting and magnifications used in routine visual inspections.	
a. Unattached foreign material on the surface of the die or within the package.	a. Unattached foreign material on the surface of the die within the package including the lid or cap.	

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
b. Unattached foreign material on the surface of the lid or cap. NOTE: Criteria of 3.2.6.1 can be satisfied by a nominal gas blow (approximately 20 psig) or a suitable cleaning process providing that the lids or caps are subsequently held in a controlled environment until capping.		
c. Attached conductive foreign material that bridges metallization paths, package leads, lead to package metallization, functional circuit elements or junctions, or any combination thereof. NOTE: Glassivated areas of the die can be excluded from the criteria of 3.2.6.1 c when the particle or material is attached only at the top surface of the glassivation.	b. Attached conductive foreign material on the top of the die and under the silox that bridges two or more metal lines. (NOTE: Attached foreign material on top of silox is not rejectable.	Vendor's criteria does not include functional circuit elements or junctions.
d. Ink on the surface of the die that covers more than 25 percent of a bonding pad area or that bridges any combination of unglassivated metallization or bare silicon area.	e. Opaque attached particles large enough to bridge any two package leads, or any lead to package metallization or a bonding pad to the edge of the die.	
	c. A clear liquid appearance on top of the silox.	
	d. Fingerprints or oily droplets	Vendor's criteria does not include all of the respective 883 criteria.
3.2.6.2 Die Mounting	3.2.7 Die Mounting (30X to 50X). No device will be acceptable which exhibits:	
a. Die mounting material buildup that extends onto the top surface of the die.	a. Die mounting material buildup that touches the top surface of the die.	
b. Die to header mounting material not visible around at least 50 percent of the die perimeter or continuous on two full sides of the die, whichever is less, except for transparent die.	b. Die to header melt not visible around 75 percent of the die perimeter and continuous on two sides.	Vendor's criteria exceeds 883B
c. Transparent die with less than 50 percent of the area bonded.		
d. Flaking of the die mounting material.		
e. Balling of the die mounting material that does not exhibit a fillet, when viewed from above (see Figure 2010-30).	c. Balling or flaking of the die mounting material.	
3.2.6.3 Die Assembly. Die not located and oriented in accordance with the applicable assembly drawing of the device.	d. Die not located or oriented in accordance with the applicable assembly drawing of the device.	
3.2.7 Glassivation Defects, "High Magnification". No device shall be acceptable that exhibits:		
a. Crazing that prohibits the detection of visual criteria contained herein.		

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

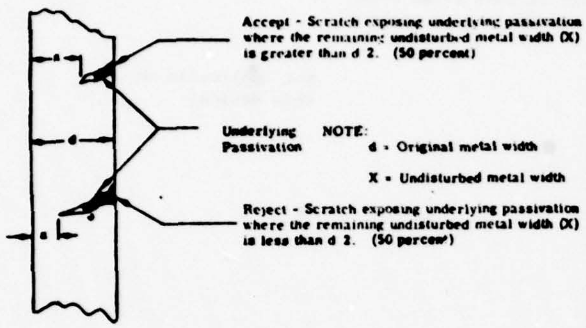
MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
b. Any lifting or peeling of the glassivation. NOTE: Lifting or peeling of the glassivation may be excluded from the criteria above, when it does not extend more than 0.001 inch distance from the designed periphery of the glassivation, provided that the only exposure of metal is of adjacent bond pads or of metallization leading from those pads.		
c. Two or more adjacent active metallization paths not covered by glassivation, excluding bonding pad cutouts.		
d. Unglassivated areas greater than 5.0 mils in any dimension, unless by design.		
e. Unglassivated areas at the edge of bonding pad exposing silicon.		
f. Glassivation covering more than 50 percent of the bonding pad area.		
g. Crazing over a film resistor.		
3.2.8 Dielectric Isolation "High Magnification". No device shall be acceptable that exhibits:		
a. A discontinous isolation line (typically a black line) around each diffusion tub containing functional circuit elements (see Figure 2010-31).		
b. Absence of a continuous isolation line between any adjacent tubs containing functional circuit elements.		
c. A diffused area which overlaps dielectric isolation material and comes closer than 0.1 mil to an adjacent diffusion tub; or an overlap of more than one diffusion area into the dielectric isolation material (see Figure 2010-31).		
d. A contact window that touches or overlaps dielectric isolation material.		
e. Metallization scratch and void defects over a dielectric isolation step shall be in accordance with criteria in 3.2.1.1 b and 3.2.1.2 b.		
	3.2.8 Package Post Metallization Defects (30X to 50X). No device shall be acceptable which appears to exhibit the following:	
	a. Post to post bridging which reduces the metallization separation to less than 25 percent.	
	b. Post voids which reduce the metallization width to less than 50 percent in the first 15 mils nearest the die.	

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences
	c. Post voids which reduce the metallization width to less than 25 percent in post areas other than the first 15 mils nearest the die.	
3.2.8 Film Resistor, "High Magnification". Rejection shall be based on defects found within the actively used portions of the film resistor. Metallization defect criteria of 3.2.1 shall apply. No device shall be acceptable that exhibits the following: a. Any misalignment between the conductor/resistor in which the actual width X of the overlap is less than 50 percent of the original resistor width (see Figure 2010-32). b. Contact overlap between the metallization and film resistor in which the length dimension Y is less than 0.25 mil (see Figure 2010-32). c. Separation between any two resistors or a resistor and a metallization path that is less than 0.1 mil, unless by design. d. Void or necking down that leaves less than 75 percent of the film resistor width undisturbed at a terminal. e. Any sharp change in the color of resistor material, within 0.1 mil of the resistor/conductor termination. f. Inactive resistor inadvertently connected to two separate points of an active circuit. g. Any thin film resistor that crosses a substrate irregularity (e.g., dielectric isolation line, oxide/diffusion step, etc.) (see figure 2010-31).		Not applicable to this device.
4. SUMMARY. The following details shall be specified in the applicable procurement document: a. Test condition (see 3). b. Where applicable, any conflicts with approved circuit design topology or construction. c. Where applicable, gages, drawings, and photographs that are to be used as standards for operator comparison (see 2). d. Where applicable, specific magnification (see 3).		

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3
Internal Visual (Monolithic)



For Multilayered Metal Products Only

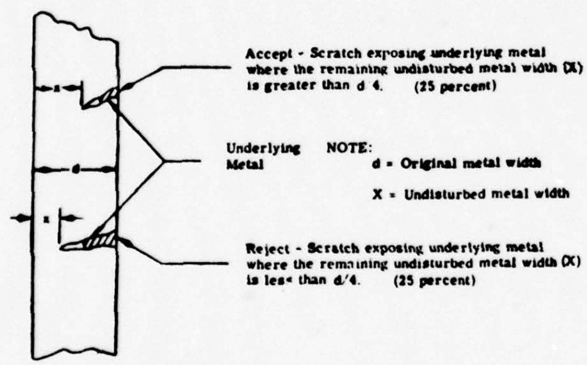


FIGURE 2010-16. SCRATCH CRITERIA

NCR Visual Inspection Criteria

SCRATCH CRITERIA

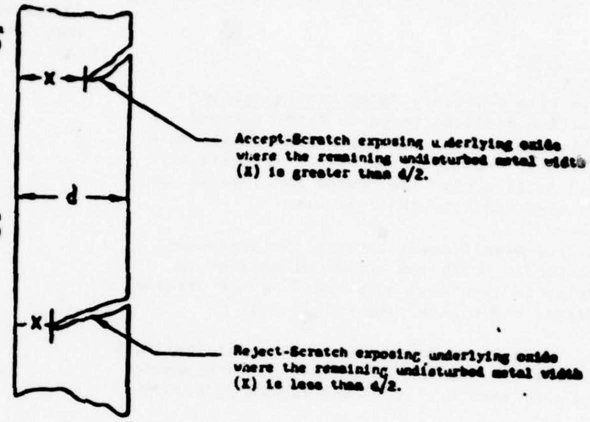
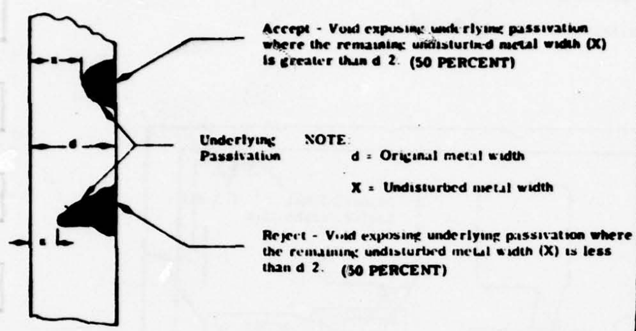


FIGURE 2

Comments/Differences

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences



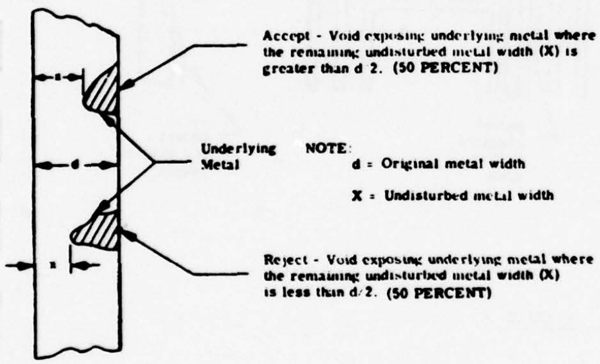


FIGURE 2010-19. VOID CRITERIA

VOID CRITERIA

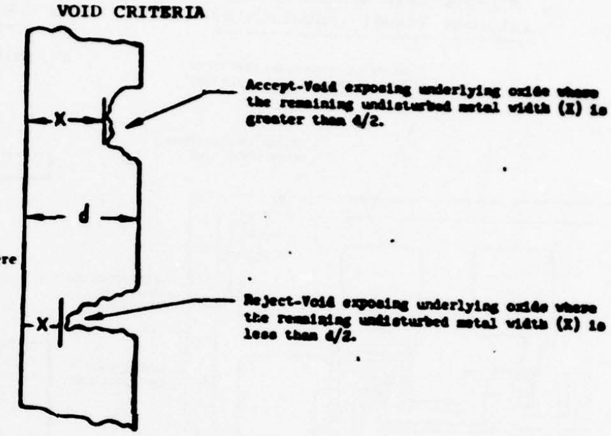


FIGURE 3

TABLE 6-1. NCR PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B Method 2010.3 Internal Visual (Monolithic)	NCR Visual Inspection Criteria	Comments/Differences

SCRIBING AND DIE DEFECTS

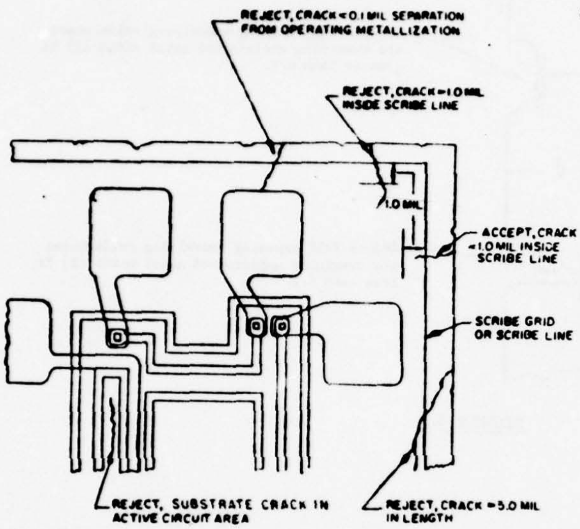


FIGURE 2010-24. SCRIBING AND DIE DEFECTS

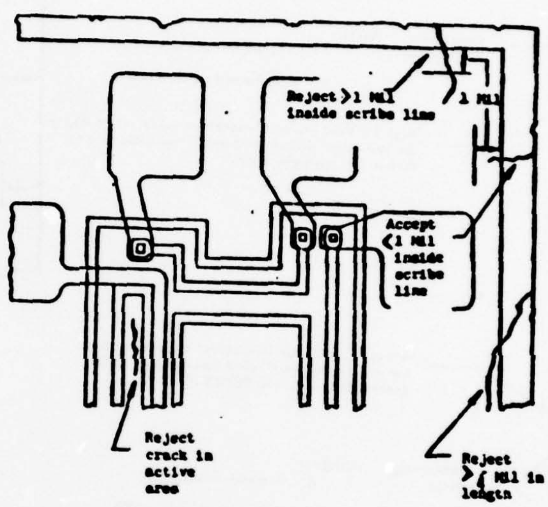


FIGURE 1

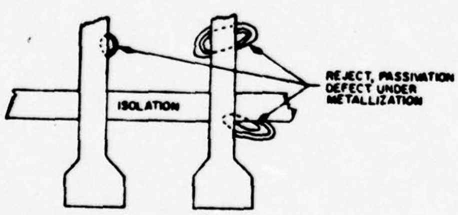
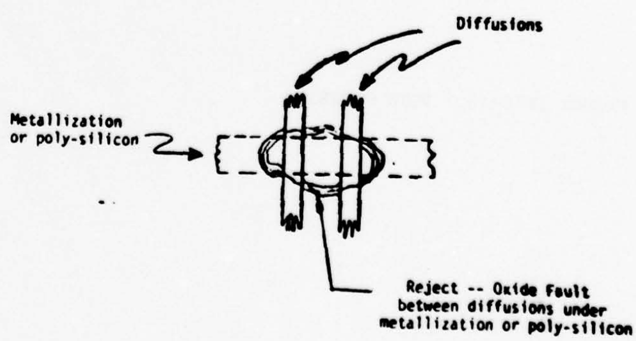


FIGURE 2010-23. PASSIVATION FAULT

OXIDE FAULTS



6.5.2 Nitron

Table 6-2 compares MIL-STD-883B and Nitron visual inspection procedures.

1079-16060

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE

MIL-STD-883B	Nitron Inspection Procedures
METHOD 2010.3	SUBJECT
INTERNAL VISUAL (MONOLITHIC)	PRESEAL QC INSPECTION (THIRD OPTICAL INSPECTION)

1. PURPOSE. The purpose of this test is to check the internal materials, construction, and workmanship of microcircuits for compliance with the requirements of the applicable procurement document. This test will normally be used prior to capping or encapsulation on a 100 percent inspection basis to detect and eliminate devices with internal defects, that could lead to device failure in normal application. It may also be employed on a sampling basis prior to capping to determine the effectiveness of the manufacturer's quality control and handling procedures for microelectronic devices. Complex microcircuits may require substitution of alternate screening procedures for visual inspection criterion pertaining to metal coverage, oxide, and diffusion faults that are difficult or impractical to perform. These alternate screening methods and procedures are documented in Method 5004, and their use shall be on an optional basis. Test condition A provides a rigorous and detailed procedure for internal visual inspection intended for high reliability class S microcircuits. Test condition B provides procedures for internal visual inspection intended for classes B and C microcircuits (classes of microcircuits refer to screening requirements of Method 5004).

2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification(s) and any visual standards (gages, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixturing shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

3. PROCEDURE.

a. General. The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the requirements of the applicable procurement document and the criteria of the specified test condition. For nonJAN devices, if a specified visual inspection requirement is in

A. SUMMARY:

This procedure describes the sample inspection of military grade product prior to final seal, following 100 percent production inspection to the same specification. The inspection criteria covers the two conditions A and B.

B. APPLICABLE TO: Quality Control

C. EQUIPMENT AND MATERIALS:

1. High power microscope, such as Bausch and Lomb binocular with vertical illumination.

   100X or 200X for condition A.

2. Low power microscope, such as Bausch and Lomb binocular, 30X to 60X.
3. Tweezers.
4. Nitrogen blow - gun.
5. Applicable product bonding diagrams.
6. Finger cots, smocks, and head coverings.
7. Laminar flow hoods.
8. Covered trays or containers.
9. QC/QA accept and reject stamps.
10. Third optical inspection report LB 4053-D (Attachment II).

E. PROCEDURE:

1. Inspection samples will be randomly picked from the total lot. Refer to Table 1 for sample size.

Comments/Differences

Procedure instructions are not directly comparable, as is inspection criteria, and therefore, is included for individual comparison

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

conflict with circuit design topology or construction, it shall be documented and specifically approved by the procuring activity. For JAN devices there shall be no waivers. The inspections and criteria in this method shall be required inspections for all devices and locations to which they are applicable. Where the criterion is intended for a specific device process or technology, it has been indicated.

b. Sequence of Inspection. The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Visual criteria specified in in 3.1.1.2, 3.1.1.5, 3.1.1.7, 3.1.2, 3.1.7e and f, 3.1.8, 3.1.9a through d, and 3.1.2.1, 3.2.1.5 3.2.1.7, 3.2.2, 3.2.7e and f, 3.2.8, 3.2.9a, b, and d may be examined prior to die attachment without required reexamination after die attachment. Visual criteria specified in 3.1.6.2, 3.1.6.3, 3.2.6.2, and 3.2.6.3 may be examined prior to bonding without reexamination after bonding. Visual criteria specified in 3.2.1.1 and 3.2.3 may be examined prior to die attachment at "high magnification" provided they are reexamined after die attachment at "low magnification." When inverted mounting techniques are employed, the inspection criteria contained herein that cannot be performed after mounting shall be conducted prior to attachment of the die.

c. Inspection Control. In all cases, examination prior to final preseal inspection shall be performed under the same quality program that is required at the final preseal inspection station. Care shall be exercised after inspections per 3b, to insure that defects created during subsequent handling will be detected and rejected at final preseal inspection. During the time interval between visual inspection and preparation for scaling, devices shall be stored in a controlled environment. Devices examined to 3.1 criteria shall be inspected and prepared for sealing in a class 100 environment and devices examined to 3.2 criteria shall be inspected and prepared for scaling in a class 100,000 environment per Federal Standard 209, except that the maximum allowable relative humidity shall not exceed 65 percent. Devices shall be in covered containers when transferred from one controlled environment to another.

d. Magnification. "High magnification" inspection shall be performed perpendicular to the die surface with the device under illumination normal to the die surface. "Low magnification" inspection shall be performed with either a monocular, binocular, or stereomicroscope, and the inspection performed within an angle of 30 degrees from the perpendicular to the die surface with the device under suitable illumination. The inspection criteria of 3.1.4, 3.2.4, and 3.2.6.1 may be examined at "high magnification" at the manufacturer's option.

Nitron Inspection Procedure

TABLE I

Lot Size	Sample Size	Accept/Reject Numbers for Different AQLs: 1%-A Criteria	2.5%-B Criteria	Other (per test plan)
Less than 90	13	0/1	0/2	(Use MIL-STD-105D, Tables I and IIA)
91 - 150	20	0/1	0/2	
151 - 280	32	1/2	2/3	
281 - 500	60	1/2	3/4	
501 - 1200	80	2/3	5/6	
1200 - 3200	125	3/4	7/8	

2. Inspect with high power settings first, then switch to low power. When inspecting at low power do not tilt the assembly being inspected more than 30 deg from the horizontal plane.

3. Refer to run card (comes with the lot) to determine which condition to use (A or B).

4. Once inspection condition has been determined turn to Inspection Criteria, Attachment I. Left side of table defines A level criteria and right side defines B level criteria.

5. Remove any defective units for reinspection by production. Defective devices must be kept away from good devices to avoid reinclusion with the lot. Mark the blade or container with the run number and the words "REJECTS".

6. Enter inspection data on third optical inspection report (form LB 4053-D) verify quantities.

7. If any question arise in applying this procedure notify your supervisor.

D. REGULATIONS:

1. Inspectors shall wear finger cots, smock, and head covering while performing third optical inspection.

2. Devices shall be in covered trays or containers when brought to the inspection station and when sent on to final seal.

3. Inspection shall be performed only under a laminar flow hood which is working properly.

4. Any material not directly required for third optical inspection will not be permitted at station.

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B	Nitron Inspection Procedure
e. Reinspection. When inspection for product acceptance or quality verification of the visual requirements herein is conducted subsequent to the manufacturer's successful inspection, the additional inspection may be performed at any magnification specified by the applicable test condition, unless a specific magnification is required by the procurement document. Where sampling is used rather than 100 percent reinspection, 6.4 of MIL-M-38510 shall apply.	
f. Exclusions. Where conditional exclusions have been allowed, specific instructions as to the location and conditions for which the exclusion can be applied shall be documented in the assembly inspection drawing.	
g. Definitions:	
1. Active circuit area includes all areas of functional circuit elements, operating metallization or any connected combinations thereof excluding beam leads.	
2. Controlled environment shall be in accordance with the requirements of Federal Standard 209 class 100 environment for air cleanliness and humidity, except that the maximum allowable relative humidity shall not exceed 50 percent. The use of an inert gas environment such as nitrogen shall satisfy the requirements for storing in controlled environment.	
3. Diffusion tub is an isolated volume of semiconductor material, either "P" or "N" type, surrounded by isolation material.	
4. Foreign material is defined as any material that is foreign to the microcircuit or any non-foreign material that is displaced from its original or intended position within the microcircuit package and shall be considered attached when it cannot be removed by a nominal gas blow (approximately 20 psig). Conductive foreign material is defined as any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection. Particles shall be considered embedded in the glassivation when there is evidence of color fringing around the periphery of the particle.	
5. Functional circuit elements are diodes, transistors, crossunders, capacitors, and resistors.	
6. Gate oxide bridge is the area lying between the drain and source diffusions of MOS structures. References to the metallization covering the gate oxide bridge shall include all materials that are used for the gate electrode.	

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

7. Glassivation is the top layer(s) of transparent insulating material that covers the active circuit area including metallization, except bonding pads and beam leads. Crazing is the presence of minute cracks in the glassivation.

8. Junction is the outer edge of a passivation step that delineates the boundary between "P" and "N" type semiconductor material.

9. Multilayered metallization (conductors) is two or more layers of metal or any other material used for interconnections that are not isolated from each other by a grown or deposited insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal.

10. Multilevel metallization (conductors) is two or more layers of metal or any other material used for interconnections that are isolated from each other by a grown or deposited insulating material.

11. Operating metallization (conductors) is all metal or any other material used for interconnection except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads, and identification markings.

12. Organic polymer (epoxy) vapor residue is the material that is emitted from the polymer, that forms on an available surface.

13. Original width is the width dimension or distance that is intended by design (e.g., original metal width, original diffusion width, original beam width, etc.).

14. Passivation step is a change in thickness of the passivation for metal to metal or metal to silicon interconnection, by design, excluding lines on the surface where passivation layers have been removed as a result of normal device processing.
attached.

'5. Passivation is the silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the deposition of metal.

16. Peripheral metal is all metal that lies immediately adjacent to or over the scribe grid.

17. Thick film is that conductive/resistive/dielectric system that is a film having greater than 50,000 angstroms thickness.

18. Thin film is that conductive/resistive/dielectric system that is a film equal to or less than 50,000 angstroms in thickness.

19. Substrate is the supporting structural material into and/or upon which the passivation, metallization and circuit elements are placed.

Nitron Inspection Procedure

F. LOT DISPOSITION:

1. Use the Accept/Reject numbers list in Table 1 to determine whether a lot is acceptable at the AQL called out in the test plan.

2. Stamp the run card and test plan sheet if applicable, with the accept or reject stamp and move the lot/paperwork to the next process location.

3. If the lot is rejected, the defective samples must be brought to the attention of the manufacturing inspector or supervisor as soon as possible and the run 100% inspected by manufacturing for the rejected defect(s) and resubmitted to QC.

G. *DEFINITIONS:*

Bond. When a wire is affixed to a bonding pad, bonding post or package termination by pressure applied impressing the wire to one of the above surfaces is a bond.

Heel. The part of the wire bond leading from the bond up off the bonding surface toward the other wire termination.

Toe. The end of the bond on the bonding pad with the tail attached.

Wire. Connects the die bond and the post bond.

Preform. Small pieces of gold that blend together when heated along with the gold on the package to bond the die down on the package.

Gold Melt. The smooth flow of preform around the die edges.

Balling and Flaking. The "GRITTY" texture of the preform that was not melted properly around the die.

Package. The part of the device on which the die is placed and wires are bonded to the leads.

Package Cavity. The deep recess in part of the package where the die is attached.

Package Leads. The gold pads or bars surrounding the top of the cavity used for placing bonds and current flows through.

H. INSPECTION CRITERIA:

See Attachment I

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

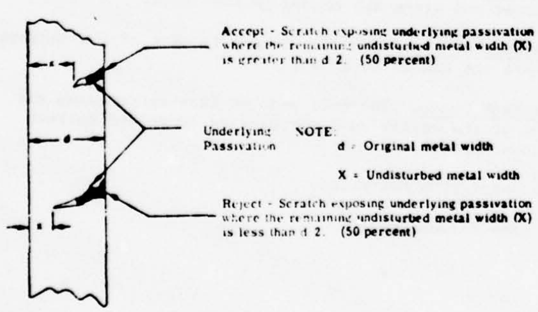
h. Interpretations. For inspections performed in the range of 75X to 100X, the criteria of "0.1 mil of passivation, separation, or metal" can be satisfied by a "line of separation" or a "line of metal." Reference herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present and shall not require confirmation by any other method of testing. When other methods of test are to be used for confirming that a reject condition does not exist, they shall be approved by the procuring activity.

3.2 TEST CONDITION B. Internal visual examination as required in 3.2.1 through 3.2.6 shall be conducted on each microcircuit and each integrated circuit chip. In addition, the applicable criteria in 3.2.7 through 3.2.9 shall be used for the appropriate microcircuits areas where glassivation, dielectric isolation or film resistors are used. The "high magnification" inspection shall be performed within the range of 75X to 150X and the "low magnification" within the range of 30X to 60X.

3.2.1 Metallization Defects "High Magnification". No device shall be acceptable that exhibits the following in the operating metallization.

3.2.1.1 Metallization Scratches. A scratch in any tearing defect, including probe marks in the surface of the metallization:

a. Scratch in the metallization excluding bonding pads, that exposes underlying passivation anywhere along its length and leaves less than 50 percent of the original metal width undisturbed (see Figure 2010-16).



b. Scratch that completely crosses a metallization path and damages the surface of the surrounding passivation on both sides. (For MOS devices, the path shall be the (L) dimension (see Figure 20.10-18).

Nitron Inspection Procedure

INSPECTION CRITERIA A

1. Metallization Defects 100X to 200X

Do not accept a scratch if more than 1/2 of metal stripe is disturbed.

Accept if less than 1/2 of metal stripe is disturbed.

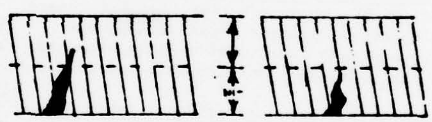


TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B	Nitron Inspection Procedure

c. Scratch in multilayered metallization that exposes the underlying metal anywhere along its length and leaves less than 25 percent of the top-layer original metal width undisturbed (see Figure 2010-16).

NOTE: Criteria of 3.2.1.1a, b, and c can be excluded for peripheral power or ground metallization where parallel paths exist such that an open at the scratch would not cause an unintended isolation of the metallization path. When application of this exclusion causes or permits a device design to exceed the current density limitation imposed by the procurement document, this exclusion shall not apply. Current density shall be determined by design not visual inspection.

For multilayered metal product only

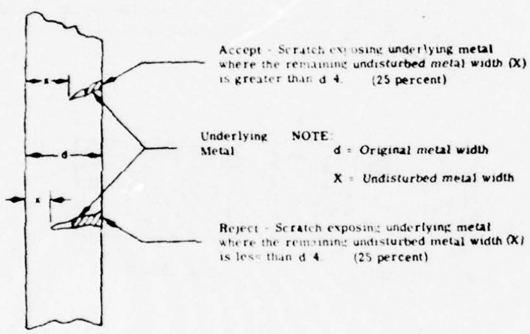


FIGURE 2010-16. SCRATCH CRITERIA

d. Scratch in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

NOTE: Criteria of 3.2.1.1a through d can be excluded for the last 25 percent of linear length of the contact cut and all metal beyond on the termination end(s) of the metallization runs. In these cases there shall be at least 50 percent of the contact opening area covered by metallization and at least a continuous 40 percent of the contact opening perimeter covered by undisturbed metallization (see Figure 2010-17).

e. Any scratch in the metallization, over the gate oxide bridge, that exposes underlying passivation and leaves less than 50 percent of the length or width of the metallization between source and drain diffusion undisturbed (see Figure 2010-18) (applicable to MOS structures).

f. Scratch in the metallization that exposes the dielectric material of a thin film capacitor or crossover.

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

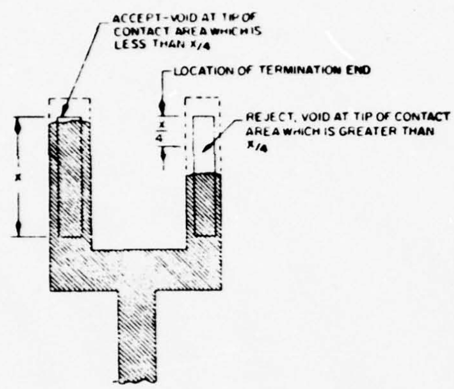
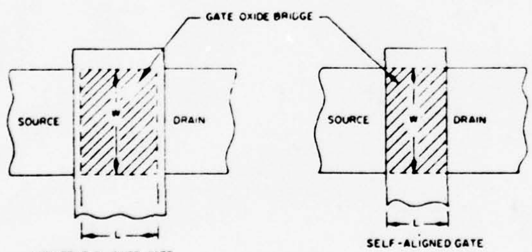


FIGURE 2010-17. TERMINATION ENDS

g. Scratch in the bonding pad or fillet area that exposes underlying passivation and reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.



NON SELF-ALIGNED GATE

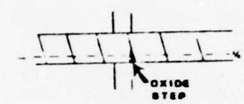
SELF-ALIGNED GATE

NOTE: When standard metallization scratch and void criterion is applied to the gate area the dimension (W) and (L) shall be considered as the original channel width and length respectively.

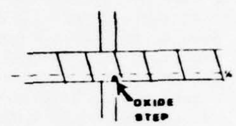
Nitron Inspection Procedure

Do not accept a scratch over an oxide step if more than 1/4 of stripe width is disturbed at the step.

Accept a scratch over an oxide step if less than 1/4 of stripe width is not disturbed at the step.



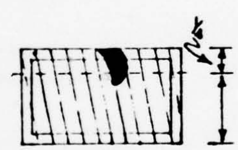
NOT ACCEPTABLE



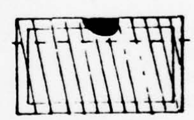
ACCEPTABLE

Do not accept if more than 1/4 of metal stripe width is disturbed over a contact edge.

Accept if less than 1/4 of metal stripe width is disturbed over a contact edge.



NOT ACCEPTABLE



ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B	Nitron Inspection Procedure

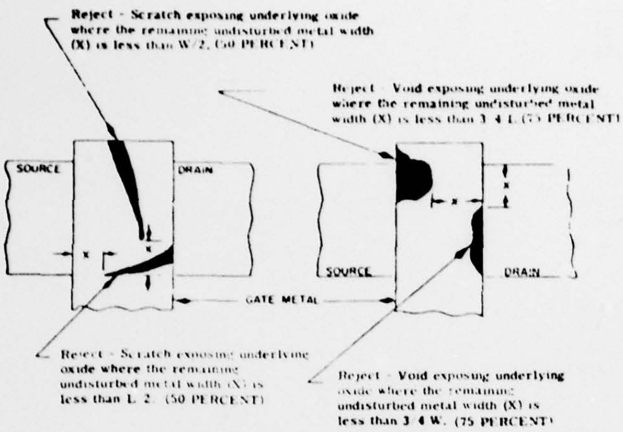
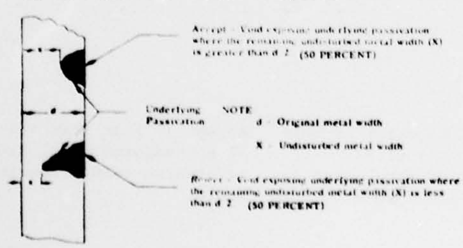


FIGURE 2010-18. MOS SCRATCH AND VOID CRITERIA

3.2.1.2 Metallization Voids. A void is any defect in the metallization where underlying metal or passivation is visible and is not caused by a scratch.

a. Void(s) in the metallization that leaves less than 50 percent of the original metal width undisturbed (see Figure 2010-19).

NOTE: Criteria of 3.2.1.2 can be excluded for peripheral power or ground metallization where parallel paths exist so that an open at the void(s) would not cause an unintended isolation of the metallization path. When application of this exclusion causes or permits a device to exceed the current density limitation imposed by the procurement document, this exclusion shall not apply. Current density shall be determined by design, not visual inspection.



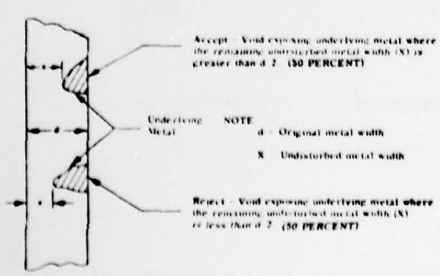


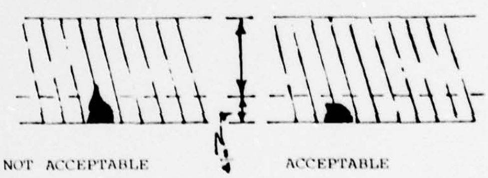
FIGURE 1020-19. VOID CRITERIA

2. Voids 100X to 200X

Do not accept if more than 1/4 of metal stripe width is disturbed.	Accept if less than 1/4 of metal width stripe is disturbed.

Comments/Differences

Vendor's criteria exceeds 883B



NOT ACCEPTABLE ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B	Nitron Inspection Procedure

b. Void(s) in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

NOTE: Criteria of 3.2.1.2a and b can be excluded for the last 25 percent of linear length of the contact cut and all metal beyond on the termination end(s) of metallization runs. In these cases there shall be at least 50 percent of contact opening area covered by metallization and at least a continuous 40 percent of the contact opening perimeter covered by undisturbed metallization (see Figure 2010-17).

c. Void(s) in the metallization over the gate oxide bridge that leaves less than 75 percent of the metallization length (L) between source and drain diffusions undisturbed (see Figure 2010-18) (applicable to MOS structures).

d. Void(s) that leave less than 60 percent of the metallization area over the gate oxide bridge undisturbed (applicable to MOS structures).

e. Void(s) that leaves less than 75 percent of the metallization width coincident with the source or drain diffusion junction line, undisturbed (see Figure 2010-18) (applicable to MOS structures).

f. Void(s) in the bonding pad area that leaves less than 75 percent of its original unglassivated metallization area undisturbed.

Do not accept if more than 1/4 of non-vapored metal area is missing from a bonding pad.

Accept if less than 1/4 of non-vapored metal area is missing from a bonding pad.

NOT ACCEPTABLE

ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

g. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width (see Figure 2010-20).

NOTE: If two or more stripes enter a bonding pad, each shall be considered separately.

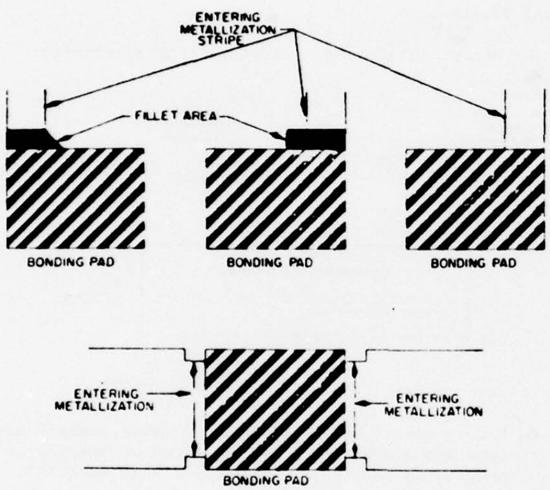


FIGURE 2010-20. BONDING PAD AREAS

h. Void(s) in the metallization of a thin film capacitor that reduces the metallization area by more than 25 percent.

3.2.1.3 Metallization Corrosion. Any metallization corrosion.

Nitron Inspection Procedure

Comments/Differences

Vendor's criteria exceeds 883B.

Do not accept missing metal in fillet area if the remaining metal is less than 3/4 of narrowest continuing stripe.

Accept missing metal in fillet area if remaining metal is more than 3/4 of narrowest continuing strip.

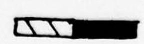
NOT ACCEPTABLE

ACCEPTABLE

Metal corrosion. Do not accept metal corrosion.

Accept if not metal corrosion.

NOT ACCEPTABLE



ACCEPTABLE

NOTE 1: Staining on bonding pads is acceptable as long as no oxide is snowing.

NOTE 2: Any die with dark brown or black discoloration on bonding pads or metal stripes shall be plated separately and submitted to supervisor.

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

3.2.1.4 Metallization Adherence. Any metallization lifting, peeling, or blistering.

Nitron Inspection Procedure

Comments/Differences

Peeling metal not covered

Metal Lifting

Do not accept metal lifting.

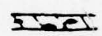
NOT ACCEPTABLE

Accept if not metal lifting.

ACCEPTABLE

Metal Blistering

Do not accept blistering metal.



NOT ACCEPTABLE

Accept if no blistering metal.

ACCEPTABLE

MIL-STD-883B

3.2.1.5 Metallization Probing. Criteria contained in 3.2.1.1 shall apply as limitations on probing damage.

3.2.1.6 Metallization Bridging. Any metallization bridging where the separation between any two metallization paths is reduced to less than 0.1 mil, unless by design.

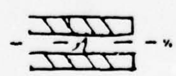
Nitron Inspection Procedure

Comments/Differences

Equivalent if metallization path width is greater than 0.2 mil

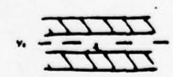
3. Bridging 100X to 200X

Do not accept if metal stripes are touching or spacing is reduced by more than 1/2.



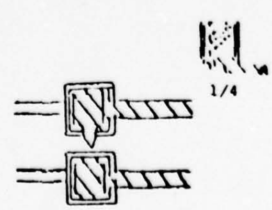
NOT ACCEPTABLE

Accept if metal stripes are not touching or spacing is reduced by less than 1/2.



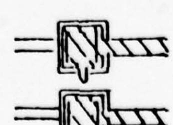
ACCEPTABLE

Do not accept a contact bridging to another contact if it comes than 1/4 of bonding pad width.



NOT ACCEPTABLE

Accept a contact bridging to another contact if it does not come closer than 1/4 of bonding pad width.



ACCEPTABLE

NOTE: If spacing between contacts is 1/4 or less of bonding pad, one visable line must be seen.

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B	Nitron Inspection Procedure

Nitron Inspection Procedure:

Do not accept excess metal that completely bridges two metalized areas or from scribeline to any metallized area.

Accept if excess metal does not completely bridge two metallized areas or from scribeline to any metallized area.

NOT ACCEPTABLE

ACCEPTABLE

MIL-STD-883B:

3.2.1.7 Metallization Alignment.

Comments/Differences
Vendor's criteria exceeds 883B.

a. Contact window that has less than 50 percent of its area covered by metallization.

Nitron Inspection Procedure:

Metal Alignment

Do not accept if 3/4 of contact area is not

Accept if 3/4 of contact area is covered by metal.

NOT ACCEPTABLE

ACCEPTABLE

MIL-STD-883B:

b. Contact window that has less than 40 percent of its perimeter covered by metallization.

NOTE: When, by design, metal is completely contained in a contact window, criteria 3.2.1.7b perimeter coverage can be deleted.

c. A metallization path not intended to cover a contact window that is separated from the window by less than 0.1 mil.

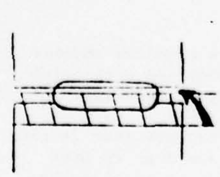
d. Any exposure of the gate oxide bridge from source to drain diffusions (see Figure 2010-21) (applicable to MOS structures).

e. Any exposure of the gate oxide bridge that leaves less than 75 percent of the metallization coincident with the source and drain diffusion junction line undisturbed (applicable to MOS structures).

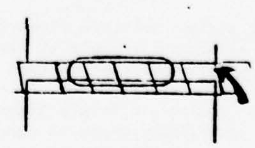
Nitron Inspection Procedure:

Do not accept if metal does not cover gate channel.

Accept if metal covers gate channel.



NOT ACCEPTABLE



ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

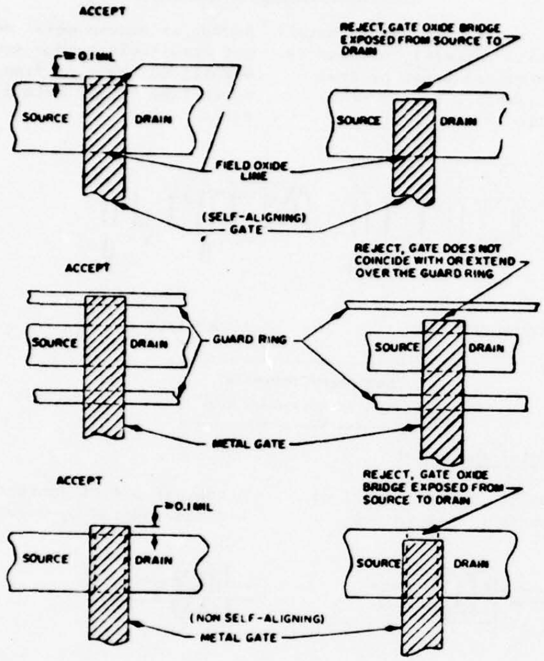


FIGURE 2010.21. MOS GATE ALIGNMENT

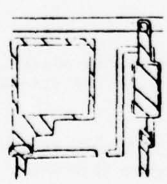
c. Either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallization (see Figure 2010-23).

NOTE: Double or triple lines indicate that it can have sufficient depth to penetrate down to bare silicon; however, should the absence of glassivation in the defect area or the characteristics of the glassivation present allow verification of the presence or absence of passivation by color or color comparisons, respectively, then these techniques may be used.

Nitron Inspection Procedure

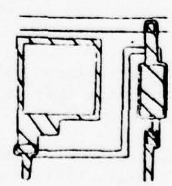
Comments/Differences
Vendor's criteria exceeds 883B.

Do not accept any broken diffusions.



NOT ACCEPTABLE

Accept if no broken diffusions.



ACCEPTABLE

Do not accept an oxide defect that bridges active metallizations.

NOT ACCEPTABLE

Accept if an oxide defect does not bridge active metallization.

ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

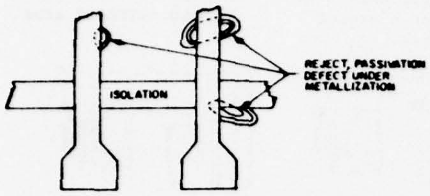


FIGURE 2010-23. PASSIVATION FAULT

Nitron Inspection Procedure

Do not accept an oxide defect along a metal edge and continuing under it.

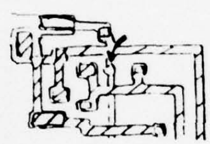
NOT ACCEPTABLE

Accept an oxide defect along a metal edge is it does not continue under it and does not have more than 1 fringe (line), 2 or more colors.

ACCEPTABLE

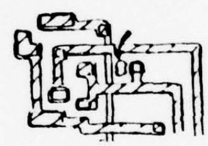
d. An active junction not covered by passivation, unless by design.

Do not accept an oxide defect in active areas.



NOT ACCEPTABLE

Accept if no oxide defects in active areas.



ACCEPTABLE

f. Gate metallization not coincident with or extending over the diffused guard ring.

NOTE: Criteria 3.2.1.7f applies to MOS structures containing a diffused guard ring. MOS devices that do not contain a diffused guard ring shall have gate metallization extending not less than 0.1 mil beyond the gate oxide bridge (see Figures 2010-18 and 2010-21).

3.2.2 Diffusion and Passivation Layer(s) Faults, "High Magnification." No device shall be acceptable that exhibits the following:

a. A diffusion junction line that unintentionally crosses another diffusion junction line (see Figure 2010-22).

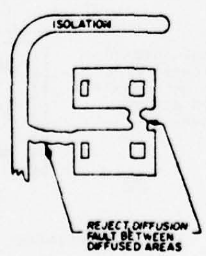
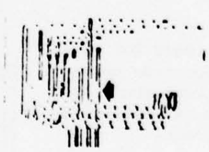


FIGURE 2010-22. DIFFUSION FAULT

Diffusion Faults

Do not accept any diffusions bridging.



NOT ACCEPTABLE

Accept if diffusions are not bridging.

ACCEPTABLE

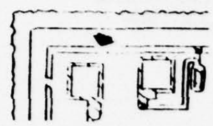
TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

b. Any isolation diffusion that is discontinuous except isolation walls around unused areas or bonding pads or any other diffused area with less than 25 percent of the original diffusion width remaining.

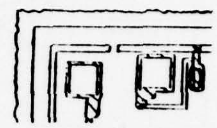
Nitron Inspection Procedure

Do not accept more than one break on a ground diffused area.



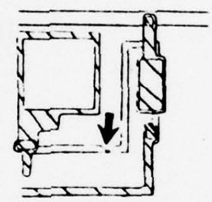
NOT ACCEPTABLE

Accept if one break on a ground diffused area.



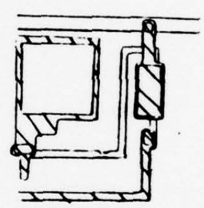
ACCEPTABLE

Do not accept any diffusion is less than 1/4 of the original area remains.



NOT ACCEPTABLE

Accept if more than 1/4 of the original area remains.



ACCEPTABLE

3.2.3 Scribing and Die Defects, High Magnification." No device shall be acceptable that exhibits:

a. Less than 0.1 mil of passivation visible between operating metallization or bond periphery and edge of the die.

NOTE: Criteria of 3.2.3a can be excluded for beam leads and peripheral metallization including bonding pads where the metallization is at the same potential as the die.

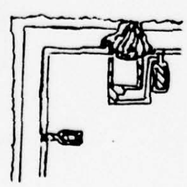
Comments/Differences

Vendor does not limit chip out size for metallization that is the same potential as the die.

b. A chipout in the active circuit area (see Figures 2010-24 and 2010-25).

NOTE: Criteria 3.2.3b can be excluded for peripheral metallization that is at the same potential as the die. In these cases there shall be at least 50 percent of the peripheral metallization width undisturbed at the chipout.

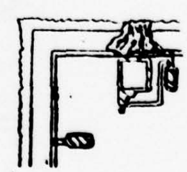
Do not accept chipouts in active areas.



NOT ACCEPTABLE

Note: Ground diffused areas are not considered active areas.

Accept a visable line between chipout and an active area.



ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

c. Any substrate or passivation crack in the active circuit area or a crack that exceeds 5.0 mils in length (see Figure 2010-24).

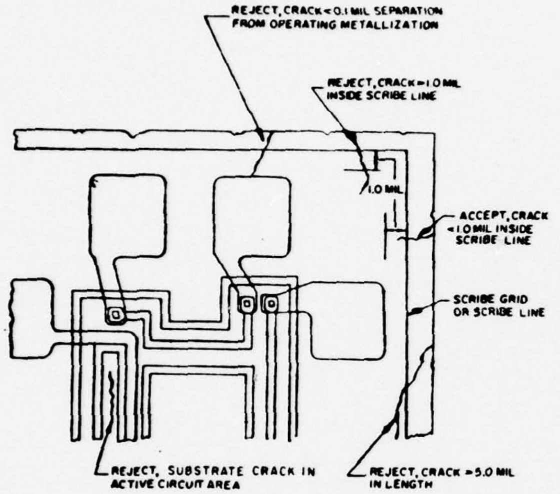
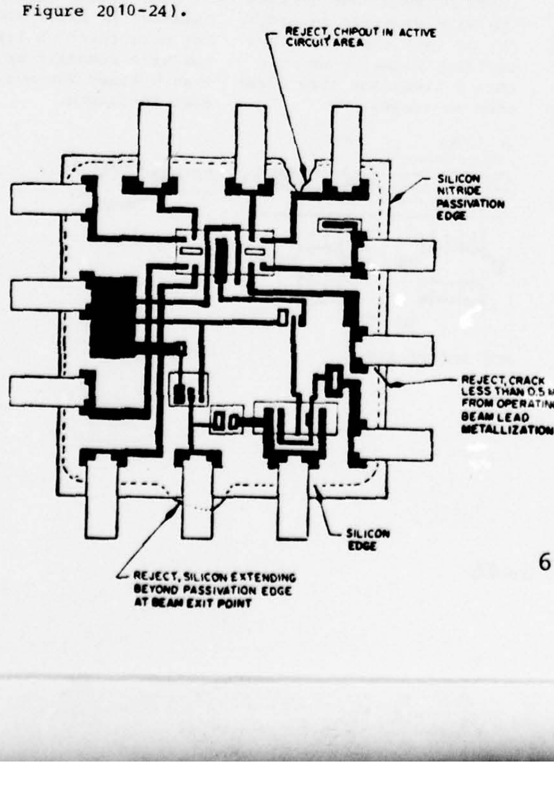


FIGURE 2010-24. SCRIBING AND DIE DEFECTS

d. Any crack that comes closer than 0.1 mil to any operating metallization or other active circuit area on the die (see Figure 2010-24).

NOTE: Criteria of 3.2.3d can be excluded for peripheral metallization that is the same potential as the die.

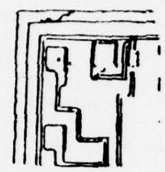
e. A crack, that exceeds 1.0 mil in length, inside the scribe grid or scribe elements (see Figure 2010-24).



Nitron Inspection Procedure

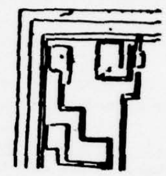
Comments/Differences
Vendor allows small cracks in active areas, otherwise equivalent if bonding pad width is less than 6.5 mils.

Do not accept a crack greater in length than 3/4 of bonding pad width.



NOT ACCEPTABLE

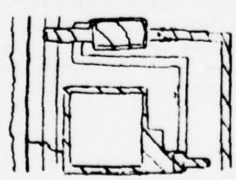
Accept a crack less than 3/4 of bonding pad width.



ACCEPTABLE

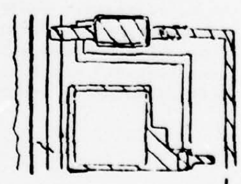
Comments/Differences
Criteria not exactly equivalent.

Do not accept a crack pointing to an active area if a distance equivalent to three visable lines cannot be seen between the crack and the active area.



NOT ACCEPTABLE

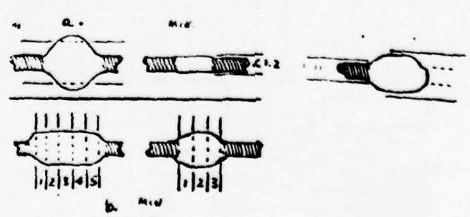
Accept a crack pointing to an active area if a distance equivalent to three visable lines can be seen between the cráck and the active area.



ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B	Nitron Inspection Procedure
f. Exposed silicon extending beyond the passivation edge at the point of the beam lead exit fromthe die (see Figure 2010-25) (applicable to beam lead structures).	
g. A crack that comes closer than 0.5 mil to operating beam lead metallization (see Figure 2010-25).	
3.2.4 Bond Inspection, "Low Magnification". This inspection and criteria shall be required for the bond type(s) to which they are applicable when viewed from above.	
NOTE: Wire tail is not considered part of the bond when determining physical bond dimensions.	
3.2.4.1 Gold Ball Bonds. No device shall be acceptable that exhibits:	
a. Gold ball bonds on the die or package post where the ball bond diameter is less than 2.0 times or greater than 6.0 times the wire diameter.	
b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.	
c. Gold ball bonds where the wire center exit is not within the boundaries of the bonding pad.	
d. Intermetallic formation extending radially more than 0.1 mil completely around the periphery of any gold ball bond for that portion of the gold ball bond located on metal.	
3.2.4.2 Wedge Bonds. No device shall be acceptable that exhibits:	Wedge Bonds
a. Ultrasonic wedge bonds on the die or package post that are less than 1.2 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 5.0 times the wire diameter in length (see Figure 2010-26).	Do not accept a bond impression less than (a) 1.2 times or more than 3 times the wire diameter in width, (b) or less than 1.5 times the wire diameter or more than 5 times the wire diameter in length. Accept a bond more than (a) 1.2 times wire diameter or less than 3 times wire diameter in width and (b) more than 1.5 times the wire diameter or less than 5 times the wire diameter in length.



NOT ACCEPTABLE ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B | Nitron Inspection Procedure

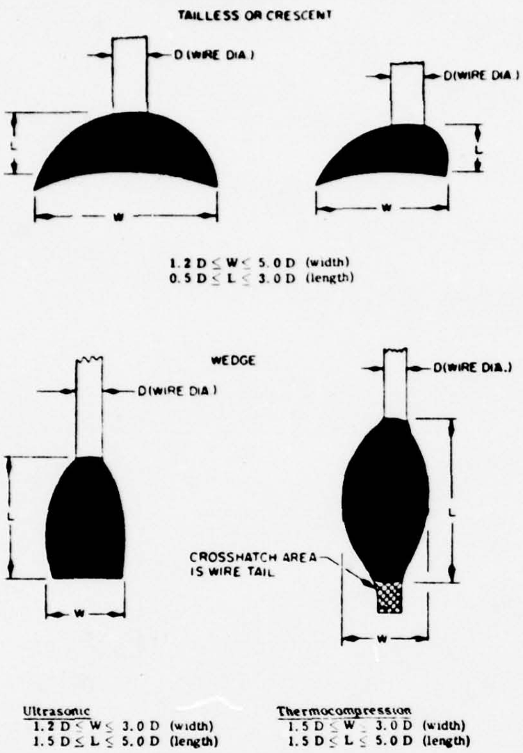


FIGURE 2010-26. BOND DIMENSIONS

b. Thermocompression wedge bonds on the die or package post that are less than 1.5 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 5.0 times the wire diameter in length (see Figure 2010-26).

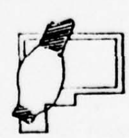
c. Wedge bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe (see Figures 2010-20 and 2010-27).

NOTES:

1. Criteria 3.2.4.2c can be excluded when the entering metallization strip is greater than 2.0 mils in width and the bond pad dimension on the entering metal stripe side is greater than 3.5 mils.

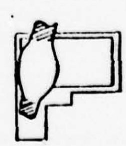
2. The requirements of 3.2.4.2c for a visual line of metal can be satisfied when an acceptable wire tail obscures the area of concern, providing the following condition exists: Bond is located more than 0.1 mil from the intersecting line of the entering metallization stripe and the bonding pad, and there is no visual evidence of disturbed pad metallization at the bond and wire tail interface.

Do not accept if a visible line of undisturbed metal cannot be seen between the bond impression and the exiting metal strip.



NOT ACCEPTABLE

Accept if a visible line of undisturbed metal can be seen between the bond impression and the exiting metal strip.



ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B	Nitron Inspection Procedure

3.2.4.3 Tailless Bonds (Crescent). No device shall be acceptable that exhibits:

a. Tailless bonds on the die or package post that are less than 1.2 times greater than 5.0 times the wire diameter in width, or are less than 0.5 times or greater than 3.0 times the wire diameter in length (see Figure 2010-26).

b. Tailless bonds where the bond impression does not cover entire width of the wire.

c. Tailless bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe (see Figure 2010-17).

3.2.4.4 General (Gold Ball, Wedge and Tailless). No device shall be acceptable that exhibits:

a. Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding pad area.

b. Bonds on the package post that are not completely within the boundaries of the package post.

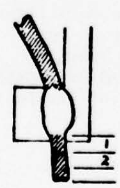
c. Bonds placed so that the wire exiting from the bond crosses over another bond.

d. Bonds placed so that the separation between bonds or the bond and operating metallization not connected to it is less than 0.1 mil.

e. Wire bond tails that extend over or make contact with any metallization not covered by glassivation and not connected to the wire.

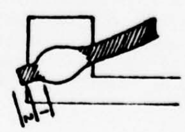
f. Wire bond tails that exceed two wire diameters in length at the bonding pad or four diameters in length at the package post.

Do not accept tails more than 2 wire diameters in length.



NOT ACCEPTABLE

Accept if tails are less than 2 wires diameters in length.



ACCEPTABLE

g. Bonds where less than 50 percent of the bond is located within an area that is free of die preform mounting material.

h. A bond on top of another bond, bond wire tail or residual segment of lead wire. An ultrasonic wedge bond alongside a previous bond where the observable width of the first bond is reduced less than 0.25 mils, is considered acceptable.

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

i. Any evidence of repair of conductors by bridging with or addition of bonding wire or ribbon.

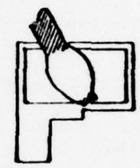
j. Any rebonding which violates the applicable rework limitations of MIL-M-38510.

Nitron Inspection Procedure

Do not accept second attempt bonding.

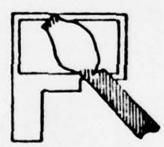
NOT ACCEPTABLE

Accept when there is not evidence of second attempt bonding.



ACCEPTABLE

Do not accept tearing at the bond heel.

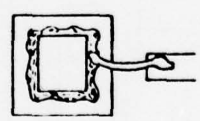


NOT ACCEPTABLE

Accept if no tearing at the bond heel.

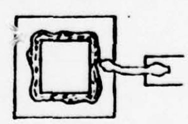
ACCEPTABLE

Do not accept ground wires bonds if more than 25% of bond impression is on die preform.



NOT ACCEPTABLE

Accept if less than 25% of the ground wire bond impression is on die preform.



ACCEPTABLE

3.2.4.5 Beam Lead. This inspection and criteria shall apply to the completed bond area made using either direct tool contact or a compliant intermediate layer. No device shall be acceptable that exhibits:

a. Bonds where the tool impression does not completely cross the entire beam width.

b. Bonds on thin film substrate metal where the tool impression increases the beam lead width less than 15 percent (10 percent for compliant bonds) or greater than 75 percent of the undeformed beam width.

c. Bonds where the tool impression length is less than 1.0 mil (see Figure 2010-28).

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B	Nitron Inspection Procedure

d. A bonding tool impression less than 1.0 mil from the die edge (see Figure 2010-29).

e. Effective bounded area less than 50 percent of that which would be possible for an exactly aligned beam (see Figure 2010-28).

f. Cracks or tears in the effective bonded area f the beam greater than 50 percent of the original beam width.

g. Bonds placed so that the separation between bonds or between bonds and operating metallization not connected to them is less than 0.1 mil.

h. Bonds lifting or peeling.

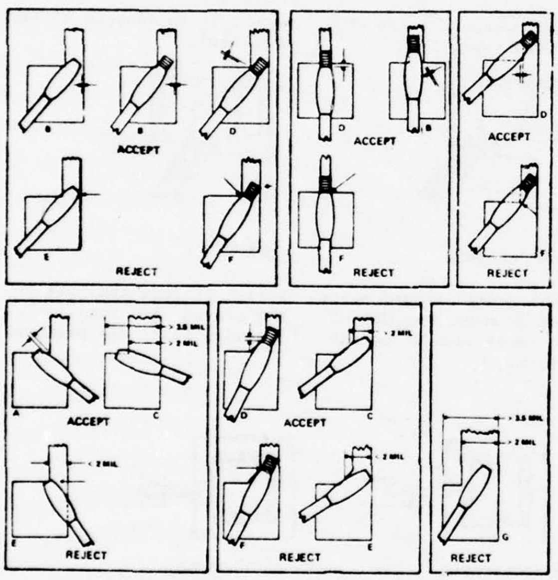
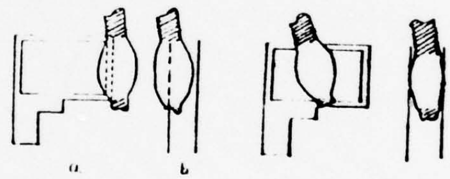


FIGURE 2010-27. BONDS AT METALLIZATION EXIT

3.2.5 Internal Leads, "Low Magnification". This inspection and criteria shall be required inspection for the lead type(s) and location(s) to which they are applicable.

Do not accept when less (a) than 75% of a bond is in the non-vapored area (of the bonding pad), (b) or when a bond on the package post is not completely within the boundaries of the package post.

Accept when (a) 75% or more of a bond is in the non-vapored area of the bonding pad (b) and when the lead bond is completely within the boundaries of the package post.



NOT ACCEPTABLE

ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

3.2.5.1 Wires. No device shall be acceptable that exhibits:

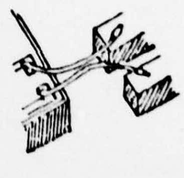
a. Any wire that touches another wire (excluding common wires), package post, unglassivated operating metallization, die, or any portion of the package.

b. Excessive loop or sag in any wire so that it comes closer than two wire diameters to another wire, package post, unglassivated operating metallization or die, or portion of the package after a spherical radial distance from the bond perimeter on the die surface of 5.0 mils for ball bonds, or 10 mils for ultrasonic and thermocompression bonds.

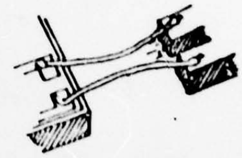
Nitron Inspection Procedure

Do not accept wires closer than 2 wire diameters to another wire, (except ground wire) package post, at any portion of the package, including the lid.

Accept wires that are more than 2 wire diameters from another wire, (except ground wire) package post, or any portion of the package, including the lid.



NOT ACCEPTABLE



ACCEPTABLE

NOTE: At 5 wire diameters from the edge of the bonding pad, the separation must be 1 wire diameter.

MIL-STD-883B

c. Nicks, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent.

Nitron Inspection Procedure

Do not accept nicks, cuts, pinched, cracking, or neckdown which reduces the wire diameter by more than 25%.

Accept wires with nicks, cuts, pinched, cracking, or neckdown, which reduce the wire diameter by less than 25%.

NOT ACCEPTABLE

ACCEPTABLE

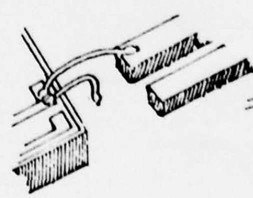
MIL-STD-883B

d. Attached extra greater than two wire diameters in length at the bonding pad or four wire diameters in length at the package post.

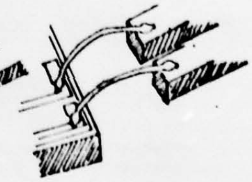
Nitron Inspection Procedure

Do not accept missing or extra lead wires.

Accept if there are no missing or extra lead wires.



NOT ACCEPTABLE



ACCEPTABLE

MIL-STD-883B

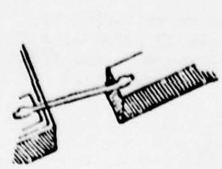
e. Tearing at the junction of the wire and bond.

f. Any wire making a straight line run from die bonding pad to package post that has no arc.

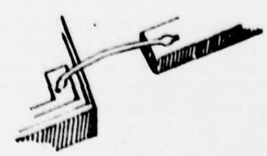
Nitron Inspection Procedure

Do not accept any wire in a straight line, with no arc (tight wires).

Accept wires with an arc.



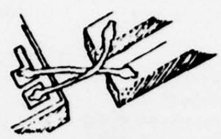
NOT ACCEPTABLE



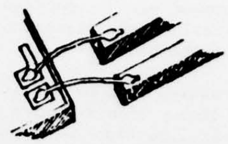
ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B	Nitron Inspection Procedure	
g. Wire(s) crossing wire(s) (except common conductors). h. Wire(s) not in accordance with bonding diagram.	Do not accept crossing wires unless from ground wire or from the same bonding pad.	Accept wires that are bonded properly.



NOT ACCEPTABLE



ACCEPTABLE

3.2.5.2 Beams. No device shall be acceptable that exhibits the following between the edge of the die and the bond area:

a. Voids, nicks, depressions, or scratches that leave less than 50 percent of the beam width undisturbed.

b. Beam separation from the die.

c. Missing or partially fabricated beam leads, unless by design.

d. Beam leads that are not bonded.

e. Bonded area closer than 0.1 mil to the edge of the passivation layer.

f. Lack of evidence of a passivation layer between the die and each beam (see Figures 2010-25 and 2010-28).

Comments/Differences
Not applicable to this device.

3.2.6 Package Conditions, "Low Magnification". No device shall be acceptable that exhibits.

3.2.6.1 Foreign Material. All foreign material or particles may be blown off with a nominal gas blow (approximately 20 psig). The device shall then be inspected and be rejected when it exhibits the following:

a. Unattached foreign material on the surface of the die or within the package.

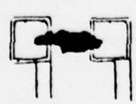
b. Unattached foreign material on the surface of the lid or cap.

NOTE: Criteria of 3.2.6.1b can be satisfied by a nominal gas blow (approximately 20 psig) or a suitable cleaning process providing that the lids or caps are subsequently held in a controlled environment until capping.

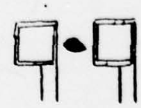
NOTE: Foreign matter is considered firmly attached if it does not remove with a nominal gas blow (20 psig).

Comments/Differences
Vendor accepts small loose foreign matter

Do not accept foreign matter large enough to bridge non-vapored areas.	Accept if foreign matter is not large enough to bridge non-vapored areas.

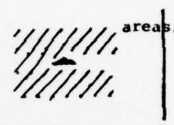


NOT ACCEPTABLE



ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B	Nitron Inspection Procedure	
c. Attached conductive foreign material that bridges metallization paths, package leads, lead to package metallization, functional circuit elements or junctions, or any combination thereof.	Do not accept foreign matter embedded in vapor than bridges metal stripes or any active areas.	Accept foreign matter embedded in vapor than does not bridge metal stripes or active areas.
NOTE: Glassivated areas of the die can be excluded from the criteria of 3.2.6.1c when the particle or material is attached only at the top surface of the glassivation.	 NOT ACCEPTABLE	 ACCEPTABLE

Comments/Differences

Vendor does not include ink that bridges metallization or silicon.

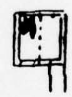
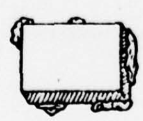
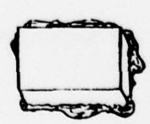
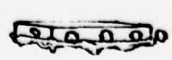
MIL-STD-883B	Nitron Inspection Procedure	
d. Ink on the surface of the die that covers more than 25 percent of a bonding pad area or that bridges any combination of unglassivated metallization or bare silicon areas.	Do not accept if more than 1/4 of bonding pad is covered with ink.  NOT ACCEPTABLE	Accept if less than 1/4 of bonding pad is covered with ink.  ACCEPTABLE
3.2.6.2 Die Mounting a. Die mounting material buildup that extends onto the top surface of the die.	Do not accept preform on die surface or if it stands higher than the die.  NOT ACCEPTABLE	Accept if preform is not on die and does not stand higher than top of the die.  ACCEPTABLE
b. Die to header mounting material not visible around at least 50 percent of the die perimeter or continuous on two full sides of the die, whichever is less, except for transparent die. c. Transparent die with less than 50 percent of the area bonded.	Do not accept if preform cannot be seen 2 complete sides or around 75% the die edge.  NOT ACCEPTABLE	Accept if die mounting material is visible around at least 2 complete sides or 75% of the die parameter.  ACCEPTABLE
d. Flaking of the die mounting material. e. Balling of the die mounting material that does not exhibit a fillet, when viewed from above (see Figure 2010-30).	Do not accept balling or flaking of die preform.  NOT ACCEPTABLE	Accept if die mounting material is smooth and exhibits no balling or flaking.  ACCEPTABLE

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B

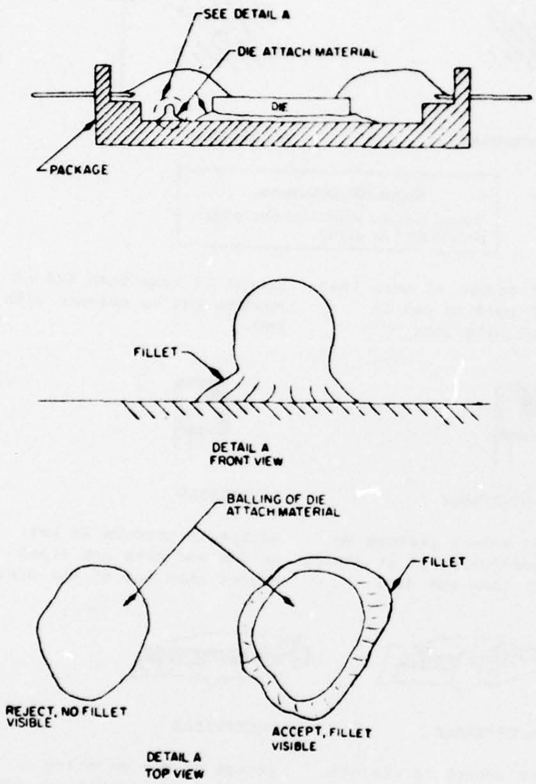
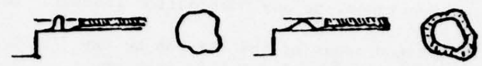


FIGURE 2010-30. BALLING OF DIE ATTACH MATERIAL

Nitron Inspection Procedure

Do not accept when preform is in peaks higher than the die surface.	Accept if preform has a smooth flow and stands lower than the die surfaces.



NOT ACCEPTABLE	ACCEPTABLE

Comments/Differences

Vendor does not include ink that bridges metallization or silicon.

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

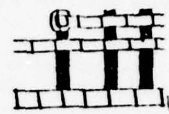
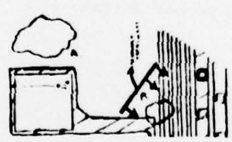
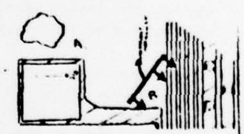
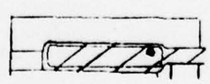
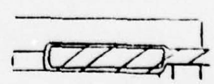
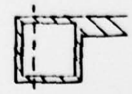
MIL-STD-883B	Nitron Inspection Procedure	
3.2.6.3 Die Assembly. Die not located and oriented in accordance with the applicable assembly drawing of the device.	Do not accept crazing vapor.	Accept if no crazing vapor.
3.2.7 Glassivation Defects, "High Magnification". No device shall be acceptable that exhibits:		
a. Crazing that prohibits the detection of visual criteria contained herein.		
b. Any lifting or pealing of the glassivation.	NOT ACCEPTABLE	ACCEPTABLE
NOTE: Lifting or pealing of the glassivation may be excluded from the criteria above, when it does not extend more than 0.001 inch distance from the designed periphery of the glassivation, provided that the only exposure of metal is of adjacent bond pads or of metallization leading from those pads.	**Comments/Differences** *Criteria not exactly equivalent.*	
c. Two or more adjacent active metallization paths not covered by glassivation, excluding bonding pad cutouts.		
d. Unglassivated areas greater then 5.0 mils in any dimension, unless by design.	Do not accept missing vapor if: (a) larger than 3/4 of bonding pad width. (b) 2 or more adjacent metallizations are not covered.	Accept missing vapor if: (a) 3/4 or smaller than bonding pad width. (b) 2 or more adjacent metallization are covered.
		
	NOT ACCEPTABLE	ACCEPTABLE
e. Unglassivated areas at the edge of bonding pad exposing silicon.	Do not accept any exposed silicon on gates.	Accept if no exposed silicon on gates.
		
	NOT ACCEPTABLE	ACCEPTABLE
f. Glassivation covering more than 50 percent of the bonding pad area.	**Comments/Differences** *Vendor's criteria exceeds 883B*	
	Do not accept vapor covering more than 1/4 of bonding pad area.	Accept if less than 1/4 of bonding pad is covered by vapor.
	 1/4	 1/4
	NOT ACCEPTABLE	ACCEPTABLE
g. Crazing over a film resistor.		

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B	Nitron Inspection Procedure
3.2.8 Dielectric Isolation, "High Magnification". No device shall be acceptable that exhibits: a. A discontinuous isolation line (typically a black line) around each diffusion tub containing functional circuit elements (see Figure 2010-31). b. Absence of a continuous isolation line between any adjacent tubs containing functional circuit elements. c. A diffused area which overlaps dielectric isolation material and comes closer than 0.2 mil to an adjacent diffusion tub; or an overlap of more than one diffusion area into the dielectric isolation material (see Figure 2010-31). d. A contact window that touches or overlaps dielectric isolation material. e. Metallization scratch and void defects over a dielectric isolation step shall be in accordance with criteria in 3.2.1.1b and 3.2.1.2b. 3.2.9 Film Resistor, "High Magnification". Rejection shall be based on defects found within the actively used portions of the film resistor. Metallization defect criteria of 3.2.1 shall apply. No device shall be acceptable that exhibits the following: a. Any misalignment between the conductor/resistor in which the actual width X of the overlap is less than 50 percent of the original resistor width (see Figure 2010-32). b. Contact overlap between the metallization and film resistor in which the length dimension Y is less than 0.25 mil (see Figure 2010-32). c. Separation between any two resistors or a resistor and a metallization path that is less than 0.1 mil, unless by design. d. Void or necking down that leaves less than 75 percent of the film resistor width undisturbed at a terminal. e. Any sharp change in the color of resistor material, within 0.1 mil of the resistor/conductor termination. f. Inactive resistor inadvertently connected to two separate points of an active circuit. g. Any thin film resistor that crosses a substrate irregularity (e.g., dielectric isolation line, oxide/diffusion step, etc.) (see Figure 2010-31).	

TABLE 6-2. NITRON PRESEAL VISUAL INSPECTION PROCEDURE (Continued)

MIL-STD-883B	Nitron Inspection Procedure	
4. <u>SUMMARY</u>. The following details shall be specified in the applicable procurement document: a. Test condition (see 3). b. Where applicable, any conflicts with approved circuit design topology or construction. c. Where applicable, gages, drawings, and photographs that are to be used as standards for operator comparison (see 2). d. Where applicable, specific magnification (see 3).	Do not accept a masking defect along a diffused junction if oxide can be seen. 	Accept a masking defect along a diffused junction if no oxide can be seen. 

6.5.3 General Instruments (GI) Quality Conformance Requirements, Class II

Table 6-3 Details the Quality Conformance Requirements of General Instruments.

TABLE 6-3. MICROELECTRONICS GROUP QUALITY CONFORMANCE REQUIREMENTS
CLASS II

GROUP - A PRODUCTION LOT SCREENING

Test	Reference MIL-STD-883 Method as Specified	GI Specification	Condition	Screen Ceramic/to Pkg. AQL	Plastic Pkg. AQL
1. Die Insp.	2010 Cond. B	QCI 30053	Production Sort Q.C. AQL	100% 1.0%	100% 1.0%
2. Wire Pull	2011 Cond. D	SPI 44503	Q.C. Audit	2X/Day	2X/Day
3. Internal Visual	2010 Cond. B	QCI 30053	Production Sort Q.C. AQL	100% 1.0%	100% 1.0%
4. Temp. Cycle	1010	QCI 31010	Production Sort Q.C. Witness Time On, Time Off	100%	100%
OR					
Temp. Shock	1011	QCI 31011	Production Sort	100%	100%
5. Herm. - Fine	1014	QCI 31014	Production Sort Q.C. AQL	100% 1.0%	NA
6. Herm. - Gross	1014	QCI 31014	Production Sort Q.C. AQL	100% 1.0%	NA
7. Elect. Test		Per Internal Test Procedure S14-xxxxx	Functional & D.C. Parametric Production Sort	100%	100%

TABLE 6-3. MICROELECTRONICS GROUP QUALITY CONFORMANCE REQUIREMENTS
CLASS II

GROUP - A PRODUCTION LOT SCREENING

Test	Reference MIL-STD-883 Method as Specified	GI Specification	Condition	Screen Ceramic/to Pkg. AQL	Plastic Pkg. AQL
8. Burn-In		Per Customer PSI	Per Customer PSI Q.C. Witness Time On, Time Off	100%	100%
9. Elect. Test (Post Burn-In)		Required only if devices are burned in	Functional & D.C. Parametric Production Sort Q.C. AQL	100% 0.65%	100% 0.65%
10. Elect. Test (Temp.		Per PSI and Test Spec. S14-xxxxx	Functional & D.C. Parametric testing (Per applicable PSI and Test Spec.) Q.C. AQL	0.65%	0.65%
11. Use Test			Per Applicable PSI Q.C. AQL	0.65%	0.65%
12. External Visual	2009	QCI 30017	Per Drawing Q.C. AQL	1.0%	1.0%
13. Packing Inspec.		QCI 30017	Q.C. AQL	1.0%	1.0%

TABLE 6-3. MICROELECTRONICS GROUP QUALITY CONFORMANCE REQUIREMENTS
CLASS II

GROUP B - PERIODIC REQUALIFICATION PROCEDURE - (EVERY THREE MONTHS PER GENERIC CATEGORY)

Test	Reference MIL-STD-883 Method as Specified	GI Specification	Condition	Screen Ceramic/to Pkg. LTPD	Plastic Pkg. LTDP
Subgroup 1					
1. Physical Dimensions	2016	QCI 30017		2 devices (no failures)	2 devices (no failures)
Subgroup 2					
1. Resistance to Solvents (Marking Durability)	2015	QCI 30017	Per Spec	5 devices (no failures)	5 devices (no failures)
2. Internal Visual Mechanical	2014	QCI 30053	Failure Criteria from design and construction requirements	1 device (no failures)	
3. Bond Strength a. Thermocompression b. Ultrasonic or wedge	2011	SPI 44503	 a. Test Condition C or D b. Test Condition C or D		
Subgroup 3					
1. Solderability	2003	QCI 31003	Soldering temperature of 260° ±10°C	15 Accept 1	15 Accept 1

TABLE 6-3. MICROELECTRONICS GROUP QUALITY CONFORMANCE REQUIREMENTS
CLASS II

GROUP C - DIE RELATED QUALIFICATIONPROCEDURE - (EVERY SIX MONTHS PER GENERIC CATEGORY)

Test	Reference MIL-STD-883 Method as Specified	GI Specification	Condition	Screen Ceramic/to Pkg. LTPD	Plastic Pkg. LTDP
Subgroup 1					
1. Operating Life Test OR HTRB	1005 1015	Per Customer PSI	Test condition to be specified (1000 hrs)	5	5
1. Endpoint Electrical		Per Internal Test Procedures S14-xxxxx	Per Group A Test 8		

TABLE 6-3. MICROELECTRONICS GROUP QUALITY CONFORMANCE REQUIREMENTS
CLASS II

GROUP D - PACKAGE RELATED QUALIFICATION PROCEDURE - (EVERY TWELVE MONTHS PER GENERIC CATEGORY)

Test	Reference MIL-STD-883 Method as Specified	GI Specification	Condition	Screen Ceramic/to Pkg. LTPD	Plastic Pkg. LTDP
Subgroup 1					
1. Physical Dimensions	2016	QCI 30017		15 Accept 1	15 Accept 1
Subgroup 2					
1. Lead Integrity	2004	QCI 31002	Test Condition B2 (lead fatigue)	15 Accept 1	15 Accept 1
2. Seal Fine Gross	1014	QCI 31014	As Applicable	15 Accept 1	N/A
Subgroup 3					
1. Thermal Shock	1011	QCI 31011	Test Condition A		
2. Temperature Cycling	1010	QCI 31010			
3. Moisture Resistance	1004	QCI 31001			
4. Pressure Cooker		QCI 30029	1 hour minimum 115°C 20PSI	N/A	
5. Seal Fine Gross	1014	QCI 31014	As Applicable	15 Accept 1	N/A

TABLE 6-3. MICROELECTRONICS GROUP QUALITY CONFORMANCE REQUIREMENTS
CLASS II

GROUP D - PACKAGE RELATED QUALIFICATION PROCEDURE - (EVERY TWELVE MONTHS PER GENERIC CATEGORY)

Test	Reference MIL-STD-883 Method as Specified	GI Specification	Condition	Screen Ceramic/to Pkg. LTPD	Plastic Pkg. LTDP
Subgroup 3 (continued)					
6. Endpoint Electrical		Per Internal Test Procedure S14-xxxxx	Per Group A Test 8	15 Accept 1	15 Accept 1
Subgroup 4 (Optional for Plastic Packages)					
1. Mechanical Shock	2002	QCI 32002			
2. Vibration Variable Frequency	2007	QCI 31000			
3. Constant Acceleration	2001	QCI 32001	Test Condition E		
4. Seal Fine Gross	1014	QCI 3014	As Applicable	15 Accept 1	N/A
5. Endpoint Electrical		Per Internal Test Procedure S14-xxxxx	Per Group A Test 8	15 Accept 1	15 Accpet 1
Subgroup 5					
1. Salt Atmosphere	1009		Test Condition A	15	

AD-A078 594 HONEYWELL INC ST PETERSBURG FLA F/G 9/2
MILITARY ADAPTATION OF COMMERCIAL ITEM (MACI) PROGRAM . -ECTR--ETC(U)
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UNCLASSIFIED 1079-16060 DELET-TR-78-2935-1 NL

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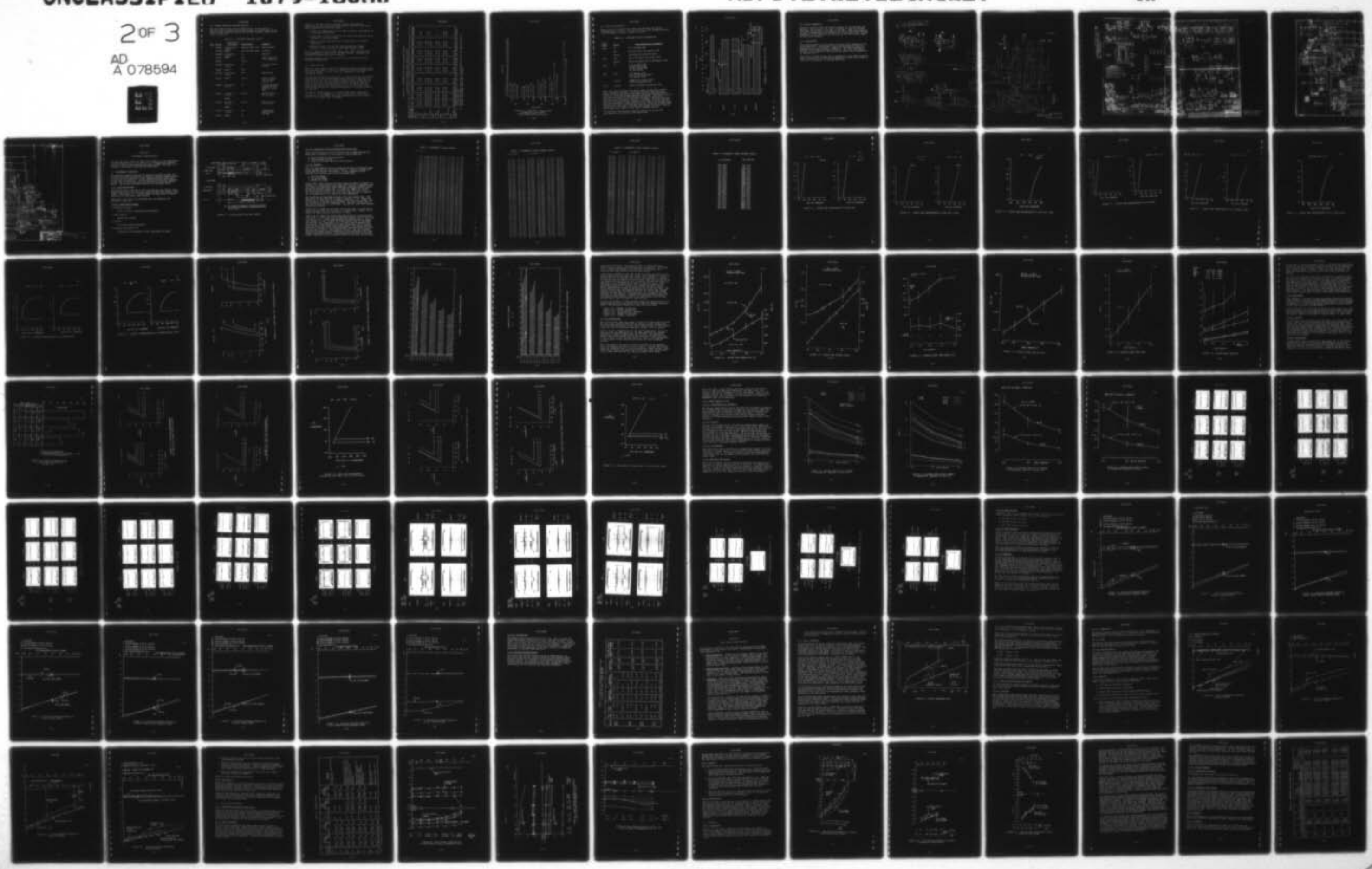
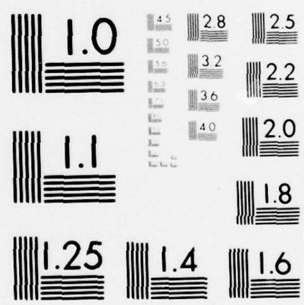




MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

6.6 VENDOR SUGGESTED CANDIDATE DEVICES

From the Vendor Survey Reports shown earlier in this section, a potential list of devices can be drawn which each manufacturer would like to become candidate devices for the MACI Program. That list is shown in Table 6-4.

TABLE 6-4. SUGGESTED CANDIDATE DEVICE

Item	Device	Organization and Type	Manufacturer	Comments
1	ER2491	1024 words X 4 bits	General Instr (GI)	Mature widely
	NCR2401	EAROM	Nat Cash Reg (NCR)	Used part
2	NCR2810	2048 wds X 4 bits	GI	New part
	ER2810	EAROM	NCR	(New revisions still appearing)
	NC2810		Nitron	
3	NCR2805	2048 wds X 4 bits	GI	Earlier Version of 2810
	ER2805	EAROM	NCR	
4	NCR2451	1024 wds X 4 bits	NCR	Mature part
	NC2451	WAROM	Nitron	Nitron production to start 4th qtr 79
5	ER3400	1024 wds X 4 bits	GI	Pin and function compatible with 2451 but faster spec
6	NC7053	128 wds X 4 bits	Nitron	Part has some partial dev.
		WAROM		
7	NC7054	256 wds X 4 bits	Nitron	Part still in partial dev.
		WAROM		
8	NCR1711	256 wds X 4 bits	NCR	Organization questionable for MACI
	ER1711	NVRAM	GI	

Several of the parts listed in Table 6-4 were eliminated by examination of the specification and initial talks with the vendors. Those eliminated are discussed below:

a. NCR/GI 1711 NVRAM would not meet MACI retention requirements of a minimum of three years.

b. NCR/GI 2805 is being replaced by the newer 2810 and will not be available in the near future.

c. ER3401 is being eliminated for the 3400 which is a similar faster part.

d. NC7054 is similar to the 7053 function but has a lower priority. Data collected on 7053 would apply to 7054.

The five remaining devices (2401, 2810, 3400, 2451, and 7053) were then considered the baseline for the MACI Program. Agreement was obtained from ERADCOM and parts ordered.

The specification sheets of each device can be obtained from the respective manufacturer.

6.7 DEVICE PRICING

Table 6-5 shows the pricing of the candidate devices as quoted 6 June 1979 from each vendor. Figure 6-1 shows the price/bit of each device type and by vendor. It also shows the comparison to GIs high reliability prices.

In analyzing the data from Figure 6-1, it can be seen that the lowest cost per bit of the available MNOS memory devices is the 2810 (8K bits) which at the 10K to 25K parts range sells for 0.104 ¢/bit and rises to 0.18 ¢/bit in small quantity (NCR). While the 2401 is a 4096 bit part or 1/2 the density of the 2810 its 10K to 25K part price rivals that of the larger part (i.e., 0.13 ¢/bit GI). This reflects the maturity of this part and points to a similar evolution for the 2810.

The 4096 bit WAROM devices (i.e., 2451, 3400) show a doubling or tripling of the 8K EAROM price reflecting the higher hierachical requirements of the WAROM, using two transistors per cell, relects a price 12 times higher than the EAROMs.

TABLE 6-5. CANDIDATE PRICE LIST (As quoted 6-6-79)

Price/Device at Quantity Level (Ceramic DIP)*

Device No. and Vendor	1-24	25-99	100-999	1000-2500	2.5K-5K	5K-10K	10K-25K	25K-100K	100K-250K
2401									
NCR	13.24	9.24	9.24	7.78	7.78	7.10	7.10	6.53	--
GI	14.00	11.00	9.00	8.00	7.00	6.50	6.00	5.00	4.75
2810									
NCR	16.00	16.00	11.17	9.40	9.40	8.58	8.58	7.89	--
GI	23.00	18.00	15.00	13.00	12.00	11.00	10.00	8.00	7.00
Nitron	24.00	21.00	18.00	16.00	16.00	16.00	14.00	14.00	--
2451									
NCR	18.90	18.90	13.20	9.40	9.40	8.58	8.58	7.89	--
Nitron	24.00	21.00	18.00	16.00	16.00	16.00	14.00	14.00	--
3400									
GI	25.00	20.00	17.00	15.00	14.00	13.00	12.00	10.00	8.50
*GI	50.00	40.00	35.00	30.00	28.00	26.00	24.00	20.00	17.00
(Hi Rel)									
7053									
Nitron	22.00	18.00	14.00	14.00	14.00	13.00	13.00	--	--

Notes: 1. Ceramic DIP prices were used since this packaging was considered most suitable for Military Use.

2. General Instruments operates a High Reliability Line for 3400 devices to MIL-883-B and temp range -40°C to +85°C.

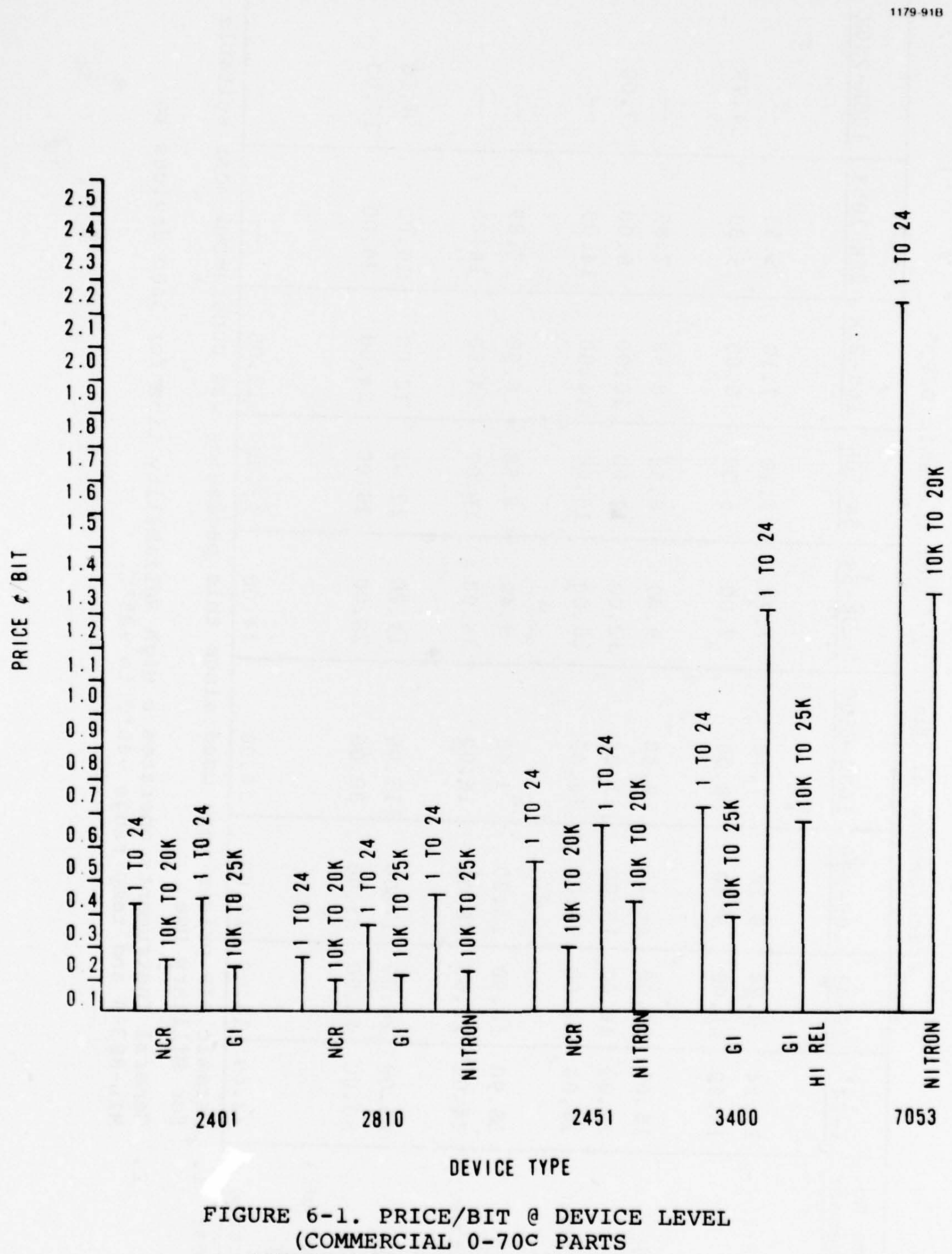


FIGURE 6-1. PRICE/BIT @ DEVICE LEVEL
(COMMERCIAL 0-70C PARTS
EXCEPT WHERE NOTED AS HI REL.)

6.8 DEVICE AVAILABILITY

While pricing is significant to most applications, the actual availability is critical. The availability of the candidate devices from the vendors is shown in Table 6-6 below:

TABLE 6-6. CANDIDATE DEVICES AVAILABILITY

Device Type	Vendor	Announced Delivery Schedule
2401	GI	8 to 10 Weeks ARO
	NCR	No parts until 4th quarter 1979
	Nitron	Not going to build this part
2451	NCR	Parts Available 4th quarter 1979
	Nitron	Parts available 3rd to 4th quarter 1979
3400	GI	8 to 10 Weeks ARO (Commercial parts) 10 to 12 Weeks ARO (Hi Rel parts)
2810	NCR	4th quarter 1979 8 to 10 Weeks starting 3rd quarter 1979
	Nitron	Samples 3rd quarter 1979 Parts 4th quarter 1979
7053	Nitron	Parts available 3rd quarter 1979

While this table reflects the quoted times for delivery of parts after receipt of an order, the actual delivery times may vary. Figure 6-2 shows the actual time parts were received after being ordered for the MACI Program preselection phase. From this it can be seen that the earliest full delivery occurred 16 weeks after ordering, with most parts received in 19 weeks. The lone exception was the 7053 which was not received by 5½ months at which time the order was cancelled. Sample devices of the 7053 were received which did not fully meet the Nitron specification in the end of March 1979. These devices were used to provide some insight into their relative performance with respect to the other candidate devices.

The 2810 was going through revisions during this period that contributed to the delivery time experienced.

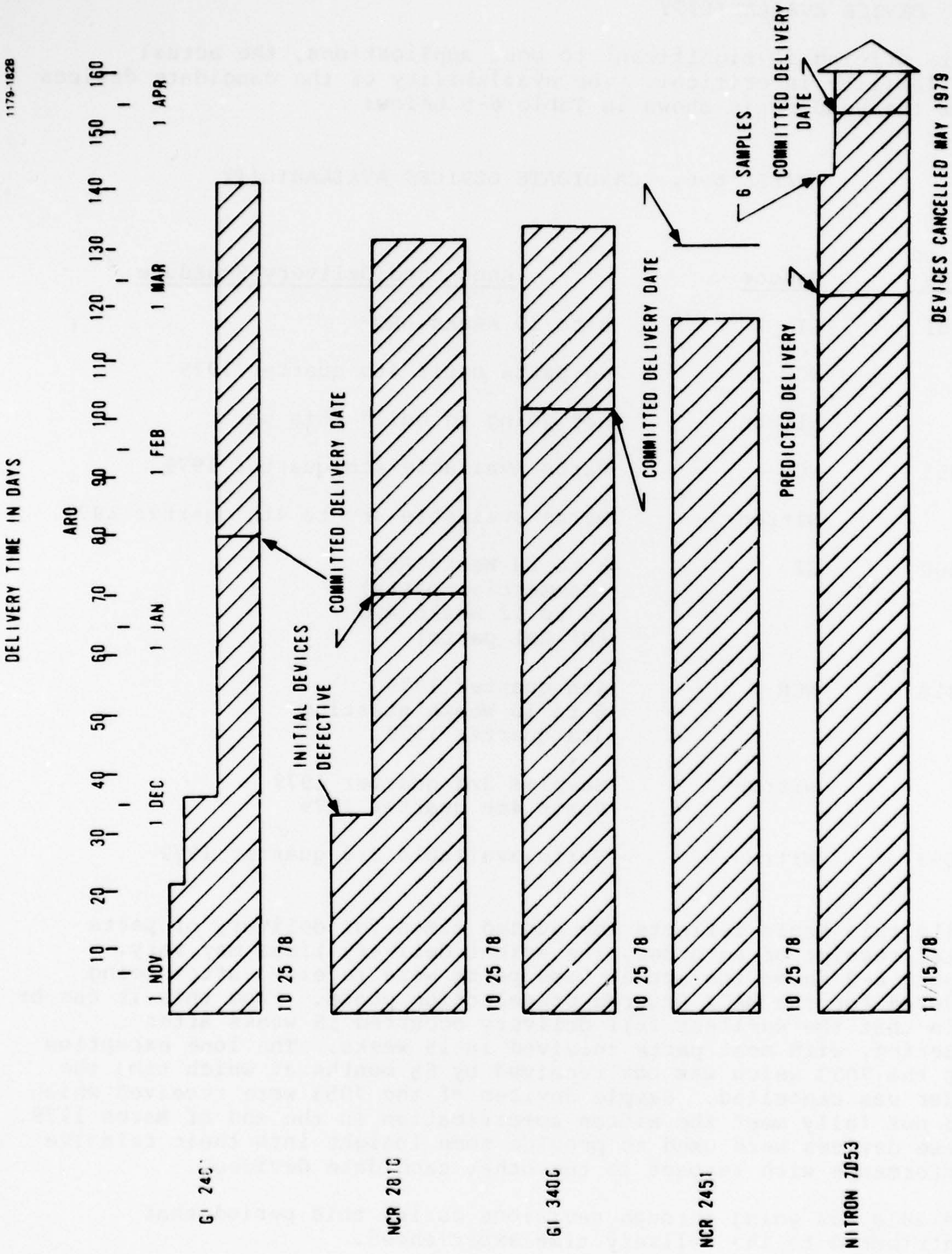


FIGURE 6-2. - DELIVERY TIME IN DAYS

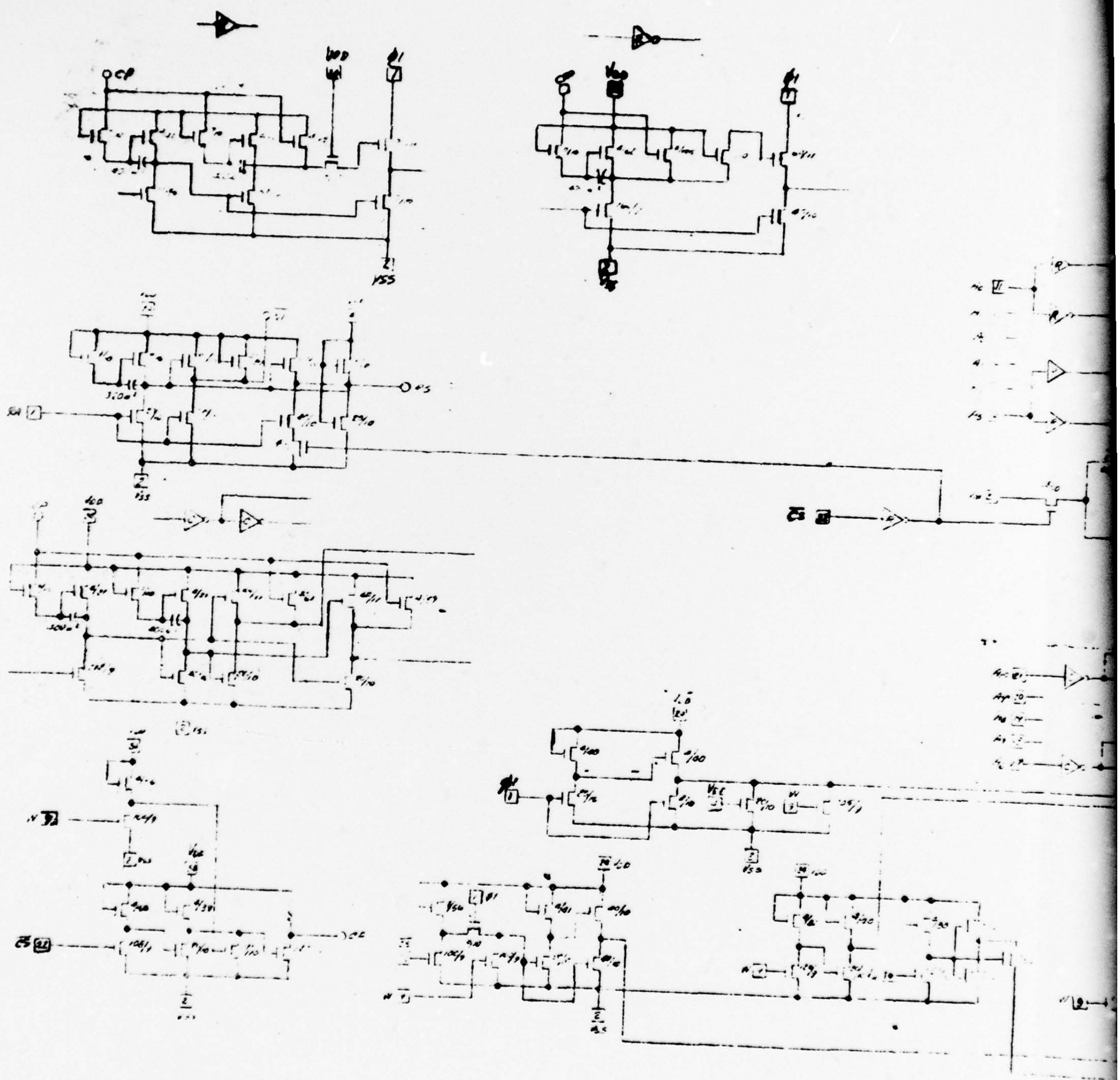
6.9 DEVICE SCHEMATICS

Figures 6-3 and 6-4 show the circuit diagrams of the 2810/2810 and the 2451. The circuit of the 2401 is similar to that of the 2810 while that of the 3400 is the same as the 2451. These were obtained to aide in understanding the operation of the devices during testing. Schematics of the 7053 were not received by the time of this report but were being shipped.

6.10 CONCLUSIONS

This section points out that there are three viable vendors for the parts identified. Several parts like the 2810 and 2451/3400 are produced by all three vendors. Support for the 2401 is waning at both NCR and GI and nonexistent at Nitron. The 7053 (and similar devices in this family) is sole sourced by Nitron with a possibility of interest by GI.

While none of these vendors can be considered a large semi-conductor house, availability of these parts appears to be low risk as long as 1985 with the exception of the 2401 and 7053.



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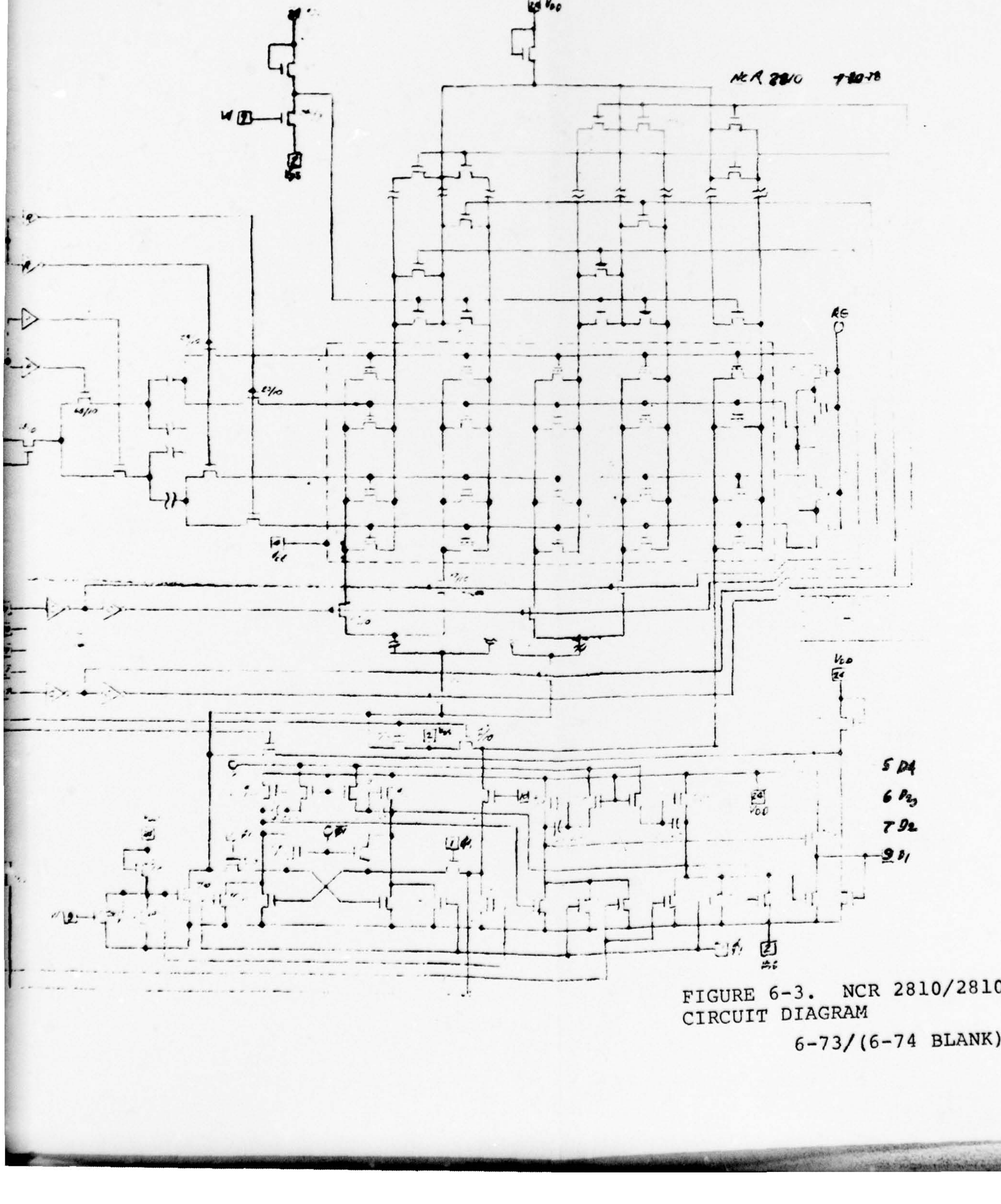
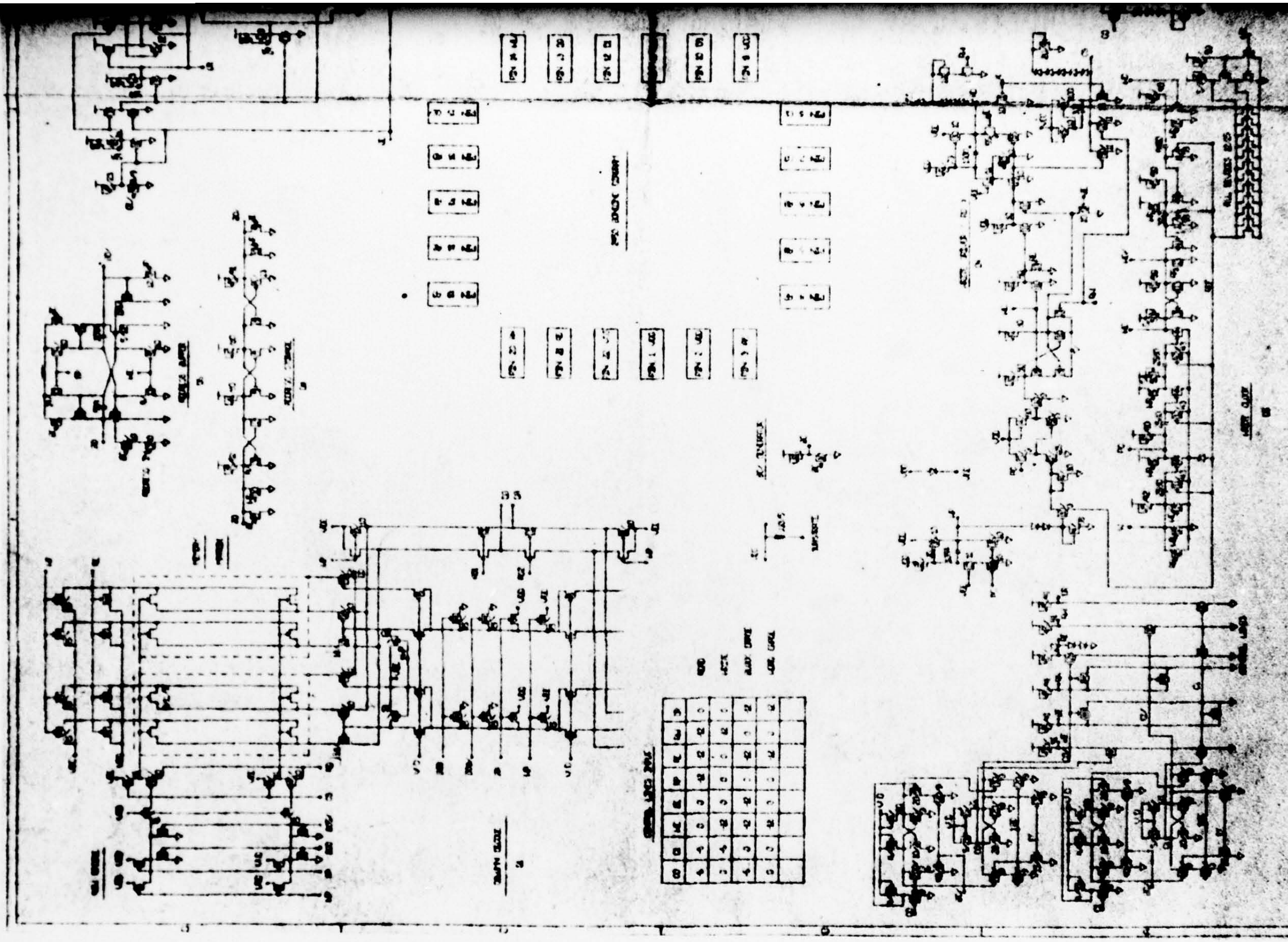


FIGURE 6-3. NCR 2810/2810
CIRCUIT DIAGRAM



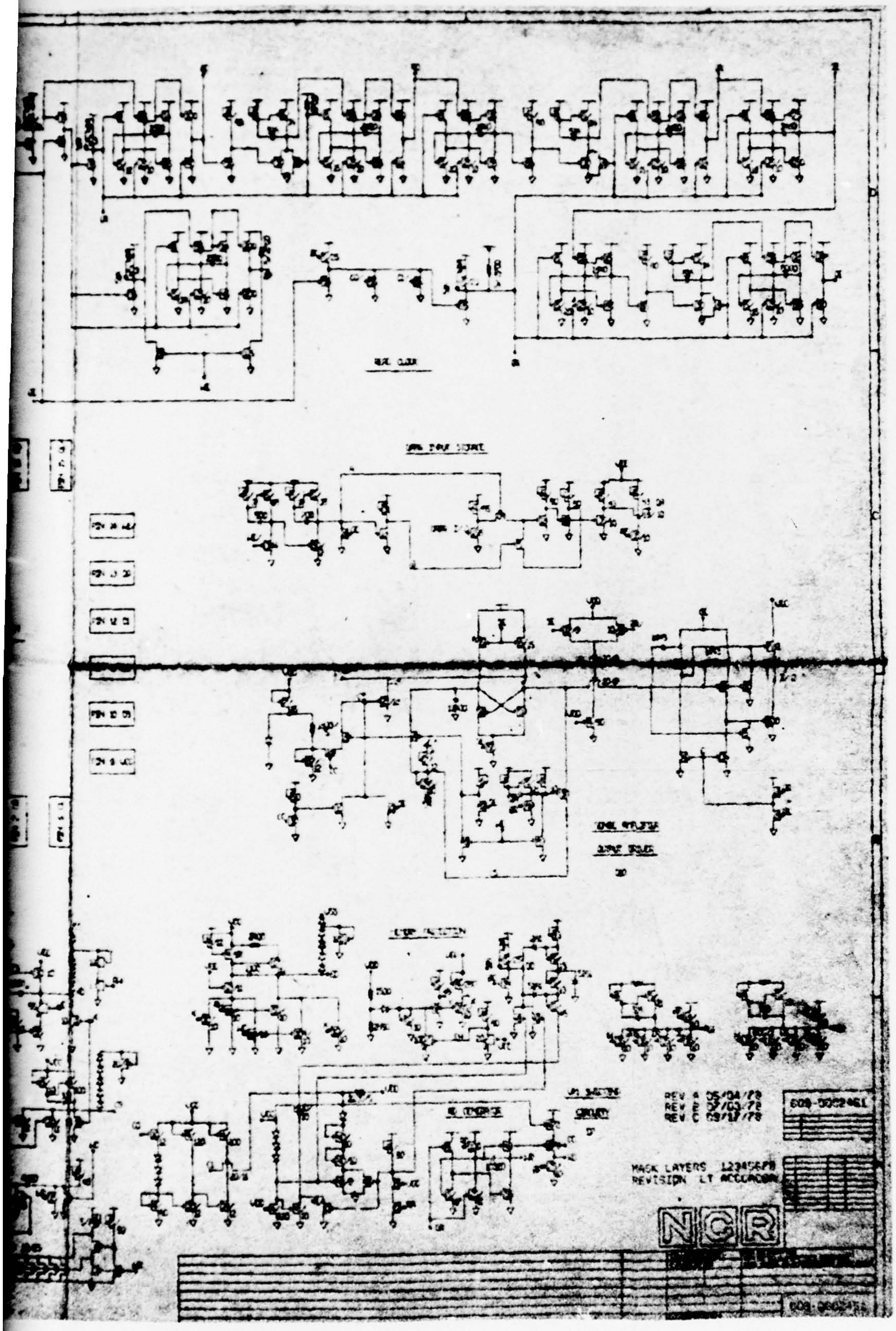
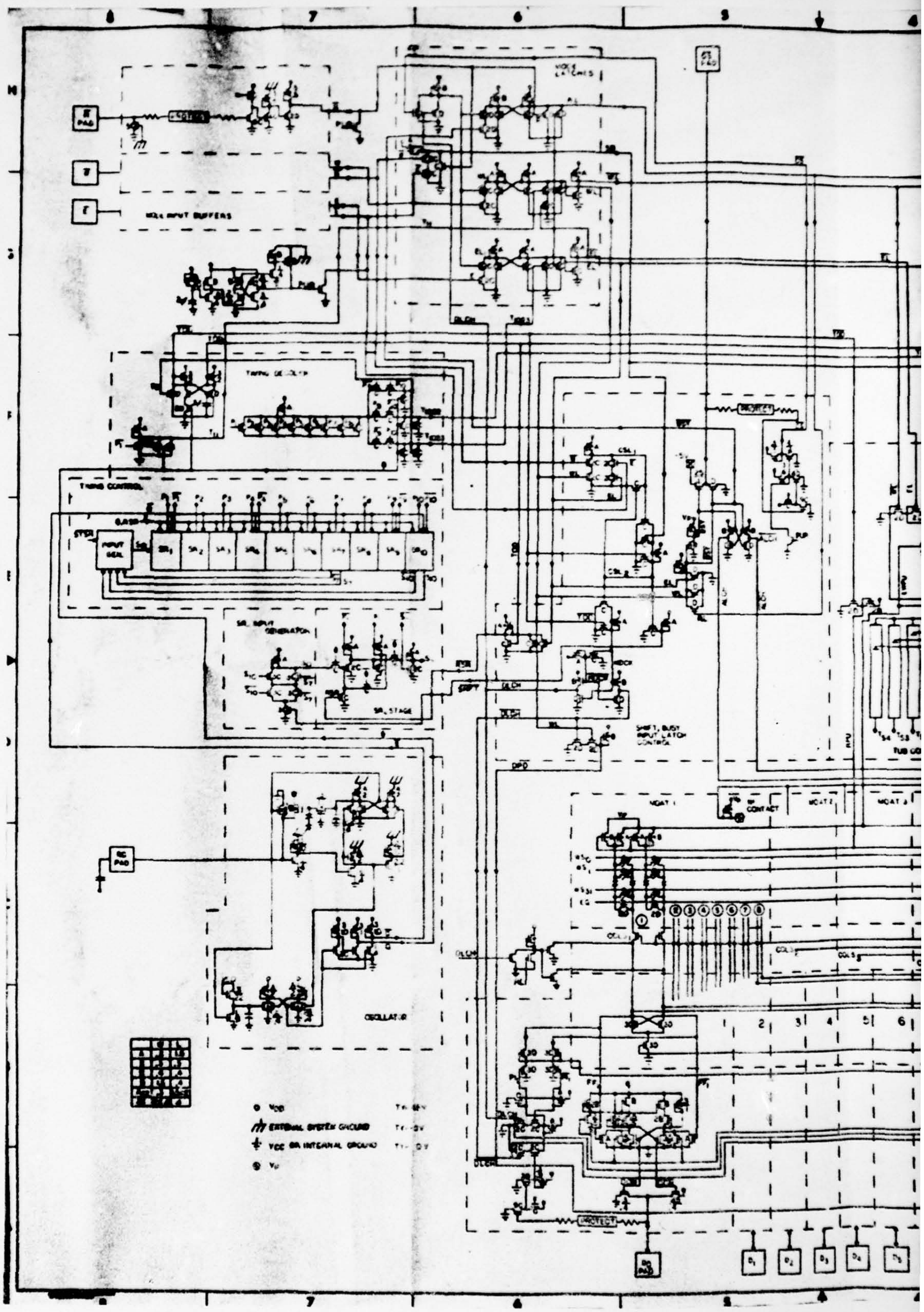


FIGURE 6-4. NCR 2451 CIRCUIT DIAGRAM



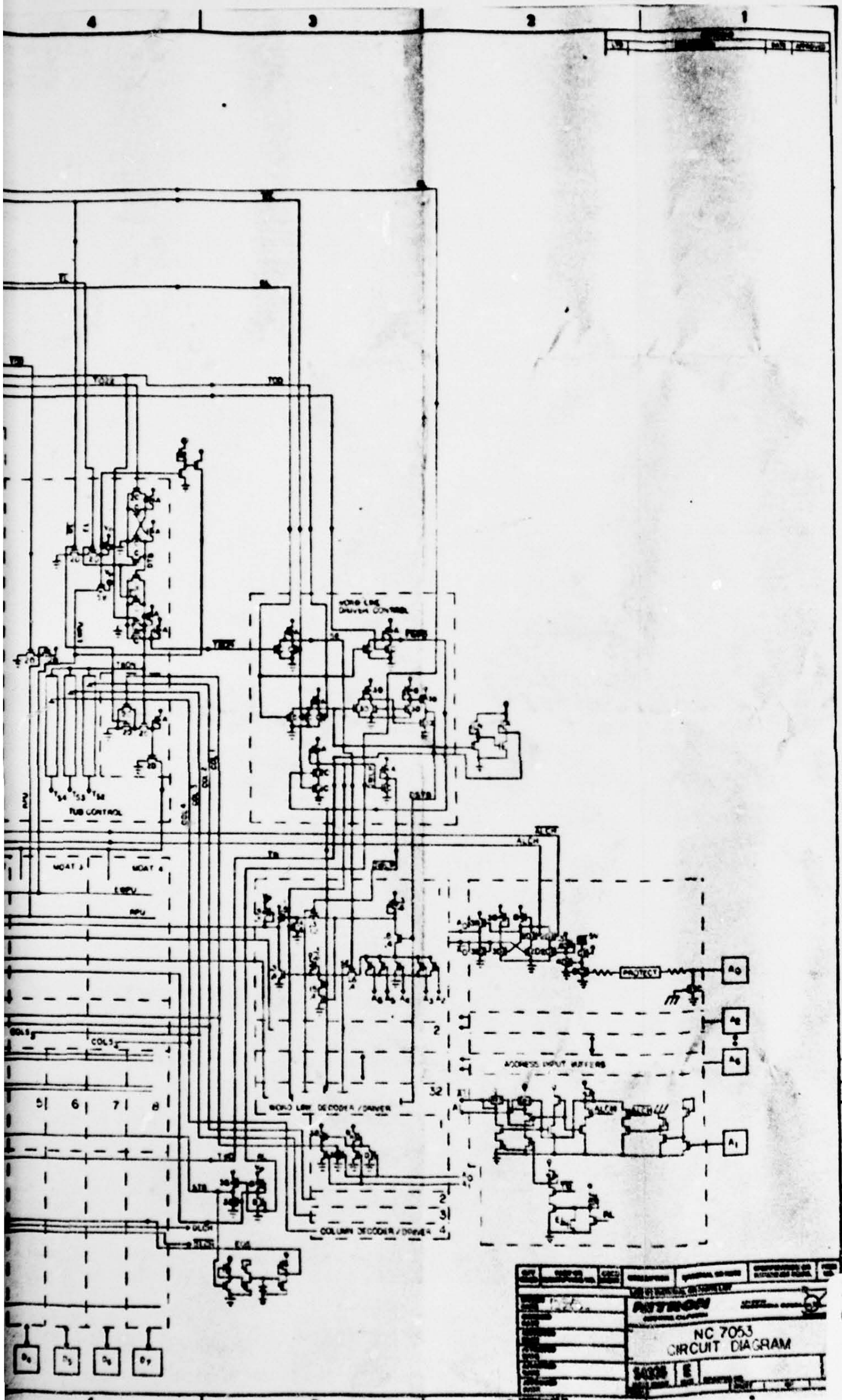


FIGURE 6-5. NITRON 7053 CIRCUIT DIAGRAM

Section 7

PERFORMANCE CHARACTERISTICS

The testing areas considered under this category are the measurement of those parameters that are common to all semiconductor memories. Section 8 covers those parameters peculiar to MNOS technology (i.e., retetion, read disturb retention and endurance).

7.1 PERFORMANCE PARAMETERS

The parameters measured during the preselection phase of MACI were selected to provide enough data to support a logical reasoned choice of the final device/devices. These measurements were split into dynamic and dc parameters. The dc parameter testing was incomplete at the time of this report and will be covered in the 2nd Interim Report. The dynamic parameters measured are discussed below.

7.1.1 Read Access Time

Read access time is defined as the time when the last address input becomes valid until the last data output becomes valid during a read cycle. (see Figure 7-1). This parameter is significant to device selection for most memory applications.

Read access time tests were conducted over and combining the following conditions.

7.1.1.1 Conditions (Tested)

a. Temperature Range:

-55°C to +125°C (Ascending and Descending)

b. Bias Voltage:

Nominal ±15 percent

c. Timing:

All timing signals optimized.

d. Patterns (See Table 7-1):

Checkerboard and Assymetric Slant (developed for MACI).

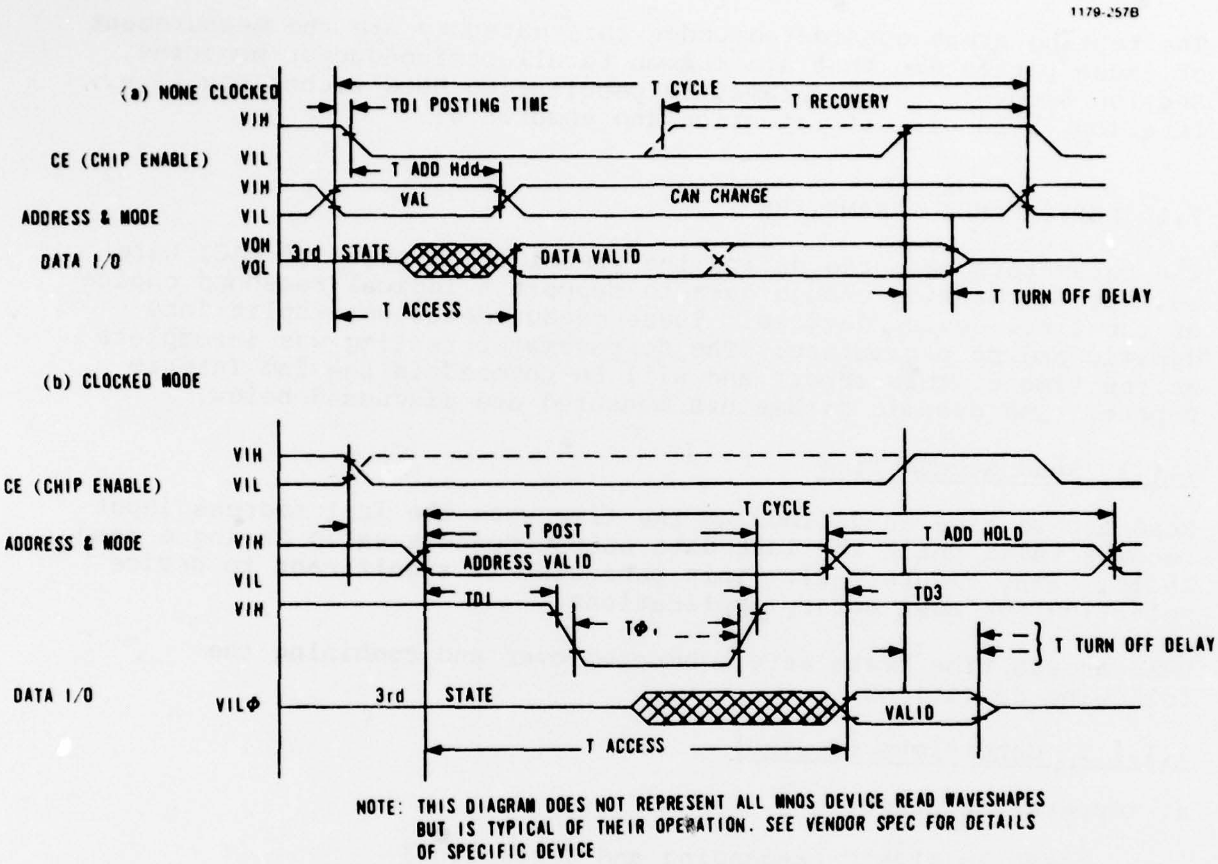


FIGURE 7-1. TYPICAL READ CYCLE WAVE SHAPES

7.1.1.2 Unmeasured Conditions Affecting Access Time

Other conditions which affect the access time of MNOS devices but which were not measured in this phase of the program are:

a. End of Retention Characteristics
b. Varied Output Loading
c. Clock and I/O Rise and Fall Time Variation

7.1.1.3 Results

Since the MACI EAROM Program is comparing devices of different types direct comparisons are not always feasible. Figure 7-2 shows both nonclocked and clocked read cycles. Of the candidate devices selected the following are of the nonclocked type:

a. NCR 2451 WAROM
b. GI ER 3400 WAROM
c. NITRON 7053 AROM

Access time characteristics for these types are shown in Figures 7-2 through 7-4. These schmoo plots show the variation in applied potential (VDD) and temperature range (ambient) and their effects on the minimum attainable access time. The abmient temperature of each device for the plots shown is; (a) -55°C, (b) -20°C, (c) +25°C, (d) +70°C and (e) +125°C. The +125°C plot for the 7053 is missing due to nonoperation of the device at that temperature.

The remaining two candidate devices are of the clocked type. The Read Cycle of these devices is shown in Figure 7-1 (b). Since the Access time of this type is a combination of TDl, Tϕl, and TD3, only the variation of TD3 was schmoo plotted. The total access time is directly proportional to this delay. TDl and Tϕl, were held constant during this testing.

Figure 7-5 (a) shows the variation of TD3 from +25° to +125°C while varying VDD from Vss -21.5 to Vss -15.9 (Vss = +5V). Figure 7-5 (b) shows this same variation from +25°C to -55°C.

Figure 7-6 (a) shows the access time characteristic of the NCR 2810 from +25°C to +125°C and over the VDD bias range at -18V to -10V (Vss -23 and Vss -15). While these diagrams are proportional to access time Figures 7-7 and 7-8 show the actual access time of the ER2401 and NCR 2810 over temperature (-55 to +125°C) and at specific VDD bias points. These diagrams also shown minimum TDl and Tϕl delays while optimizes the access time measurements. The results shown in Figures 7-2 through 7-8 illustrate typical characteristics of individual devices of each of the candidate devices. The use of schmoo plotting techniques allows examination of the continuous bias range access time characteristics. By performing these plots at selected ambient temperature points optimum biasing for use over the military

TABLE 7-1. ASSYMETRIC SLANT PATTERN

LOC	CONTENTS	LOC	CONTENTS	LOC	CONTENTS	LOC	CONTENTS	LOC	CONTENTS	LOC	CONTENTS
0	1011	54	0110	108	1011	162	1011	216	1101	270	1101
1	0110	55	1101	109	0110	163	0110	217	1010	271	1011
2	1101	56	1101	110	1101	164	1101	218	0101	272	0110
3	1011	57	1011	111	1011	165	1011	219	1011	273	1101
4	0110	58	0110	112	0110	166	0110	220	0110	274	1011
5	1101	59	1101	113	1101•	167	1101	221	1101	275	0110
6	1011	60	1011	114	1011	168	1011	222	1011	276	1101
7	0110	61	0110	115	0110	169	0110	223	0110	277	1011
8	1101	62	1101	116	0110	170	1101	224	1101	278	0110
9	1011	63	1011	117	1101	171	1011	225	1011	279	1101
10	0110	64	0110	118	1010	172	0110	226	0110	280	1011
11	1101	65	1101	119	0101	173	1101	227	1101	281	0110
12	1011	66	1011	120	1011	174	1011	228	1011	282	1101
13	0110	67	0110	121	0110	175	0110	229	0110	283	1010
14	1101	68	1101	122	1101	176	0110	230	1101	284	0101
15	1011	69	1011	123	1011	177	1101	231	1011	285	1011
16.	0110	70	0110	124	0110	178	1011	232	0110	286	0110
17	1101	71	1101	125	1101	179	0110	233	1101	287	1101
18	1010	72	1011	126	1011	180	1101	234	1011	288	1011
19	0101	73	0110	127	0110	181	1011	235	0110	289	0110
20	1011	74	1101	128	1101	182	0110	236	0110	290	1101
21	0110	75	1011	129	1011	183	1101	237	1101	291	1011
22	1101	76	0110	130	0110	184	1010	238	1011	292	0110
23	1011	77	1101	131	1101	185	0101	239	0110	293	1101
24	0110	78	1011	132	1011	186	1011	240	1101	294	1011
25	1101	79	0110	133	0110	187	0110	241	1011	295	0110
26	1101	80	1101	134	1101	188	1101	242	0110	296	0110
27	1011	81	1011	135	1011	189	1011	243	1101	297	1101
28	0110	82	0110	136	0110	190	0110	244	1011	298	1011
29	1101	83	1101	137	1101	191	1101	245	0110	299	0110
30	1011	84	1010	138	1011	192	1011	246	1101	300	1101
31	0110	85	0101	139	0110	193	0110	247	1011	301	1011
32	1101	86	0101	140	1101	194	1101	248	0110	302	0110
33	1011	87	1011	141	1011	195	1011	249	1101	303	1101
34	0110	88	0110	142	0110	196	0110	250	1010	304	1011
35	1101	89	1101	143	1101	197	1101	251	0101	305	0110
36	1011	90	1011	144	1011	198	1011	252	1011	306	1101
37	0110	91	0110	145	0110	199	0110	253	0110	307	1011
38	1101	92	1101	146	0110	200	1101	254	1101	308	0110
39	1011	93	1011	147	1101	201	1011	255	1011	309	1101
40	0110	94	0110	148	1011	202	0110	256	0110	310	1011
41	1101	95	1101	149	0110	203	1101	257	1101	311	0110
42	1011	96	1011	150	1101	204	1011	258	1011	312	1101
43	0110	97	0110	151	1010	205	0110	259	0110	313	1011
44	1101	98	1101	152	0101	206	0110	260	1101	314	0110
45	1011	99	1011	153	1011	207	1101	261	1011	315	1101
46	0110	100	0110	154	0110	208	1011	262	0110	316	1010
47	1101	101	1101	155	1101	209	0110	263	1101	317	0101
48	1011	102	1011	156	1011	210	1101	264	1011	318	1011
49	0110	103	0110	157	0110	211	1011	265	0110	319	0110
50	1101	104	1101	158	1101	212	0110	266	0110	320	1101
51	1010	105	1011	159	1011	213	1101	267	1101	321	1011
52	0101	106	0110	160	0110	214	1011	268	1011	322	0110
53	1011	107	1101	161	1101	215	0110	269	0110	323	1101

TABLE 7-1. ASSYMETRIC SLANT PATTERN (CONT'D)

LOC	CONTENTS	LOC	CONTINTS								
324	1011	378	1101	432	1101	486	1101	540	0110	594	1101
325	0110	379	1011	433	1011	487	1011	541	1101	595	1011
326	0110	380	0110	434	0110	488	0110	542	1011	596	1011
327	1101	381	1101	435	1101	489	1101	543	0110	597	0110
328	1011	382	1010	436	1011	490	1011	544	1101	598	1101
329	0110	383	0101	437	0110	491	0110	545	1011	599	1011
330	1101	384	1011	438	1101	492	1101	546	0110	600	0110
331	1011	385	0110	439	1011	493	1011	547	1101	601	1101
332	0110	386	0110	440	0110	494	0110	548	1010	602	1011
333	1101	387	1101	441	1101	495	1101	549	0101	603	0110
334	1011	388	1011	442	1011	496	1011	550	1011	604	1101
335	0110	389	0110	443	0110	497	0110	551	0110	605	1011
336	1101	390	1101	444	1101	498	1101	552	1101	606	0110
337	1011	391	1011	445	1011	499	1011	553	1011	607	1101
338	0110	392	0110	446	1011	500	0110	554	0110	608	1011
339	1101	393	1101	447	0110	501	1101	555	1101	609	0110
340	1011	394	1011	448	1101	502	1011	556	1011	610	1101
341	0110	395	0110	449	1010	503	0110	557	0110	611	1011
342	1101	396	1101	450	0101	504	1101	558	1101	612	0110
343	1011	397	1011	451	1011	505	1011	559	1011	613	1101
344	0110	398	0110	452	0110	506	1011	560	0110	614	1010
345	1101	399	1101	453	1101	507	0110	561	1101	615	0101
346	1011	400	1011	454	1011	508	1101	562	1011	616	1011
347	0110	401	0110	455	0110	509	1011	563	0110	617	0110
348	1101	402	1101	456	1101	510	0110	564	1101	618	1101
349	1010	403	1011	457	1011	511	1101	565	1011	619	1011
350	0101	404	0110	458	0110	512	1011	566	1011	620	0110
351	1011	405	1101	459	1101	513	0110	567	0110	621	1101
352	0110	406	1011	460	1011	514	1101	568	1101	622	1011
353	1101	407	0110	461	0110	515	1010	569	1011	623	0110
354	1011	408	1101	462	1101	516	0101	570	0110	624	1101
355	0110	409	1011	463	1011	517	1011	571	1101	625	1011
356	0110	410	0110	464	0110	518	0110	572	1011	626	1011
357	1101	411	1101	465	1101	519	1101	573	0110	627	0110
358	1011	412	1011	466	1011	520	1011	574	1101	628	1101
359	0110	413	0110	467	0110	521	0110	575	1011	629	1011
360	1101	414	1101	468	1101	522	1101	576	0110	630	0110
361	1011	415	1010	469	1011	523	1011	577	1101	631	1101
362	0110	416	1010	470	0110	524	0110	578	1011	632	1011
363	1101	417	0101	471	1101	525	1101	579	0110	633	0110
364	1011	418	1011	472	1011	526	1011	580	1101	634	1101
365	0110	419	0110	473	0110	527	0110	581	1010	635	1011
366	1101	420	1101	474	1101	528	1101	582	0101	636	0110
367	1011	421	1011	475	1011	529	1011	583	1011	637	1101
368	0110	422	0110	476	1011	530	0110	584	0110	638	1011
369	1101	423	1101	477	0110	531	1101	585	1101	639	0110
370	1011	424	1011	478	1101	532	1011	586	1011	640	1101
371	0110	425	0110	479	1011	533	0110	587	0110	641	1011
372	1101	426	1101	480	0110	534	1101	588	1101	642	0110
373	1011	427	1011	481	1101	535	1011	589	1011	643	1101
374	0110	428	0110	482	1010	536	1011	590	0110	644	1011
375	1101	429	1101	483	0101	537	0110	591	1101	645	0110
376	1011	430	1011	484	1011	538	1101	592	1011	646	1101
377	0110	431	0110	485	0110	539	1011	593	0110	647	1010

TABLE 7-1. ASSYMETRIC SLANT PATTERN (CONT'D)

LOC	CONTENTS			LOC.	CONTENTS						
648	0101	702	0110	756	0110	810	1011	864	0110	918	0110
649	1011	703	1101	757	1101	811	0110	865	1101	919	1101
650	0110	704	1011	758	1011	812	1101	866	1101	920	1011
651	1101	705	0110	759	0110	813	1010	867	1011	921	0110
652	1011	706	1101	760	1101	814	0101	868	0110	922	1101
653	0110	707	1011	761	1011	815	1011	869	1101	923	1011
654	1101	708	0110	762	0110	816	0110	870	1011	924	0110
655	1011	709	1101	763	1101	817	1101	871	0110	925	1101
656	1011	710	1011	764	1011	818	1011	872	1101	926	1101
657	0110	711	0110	765	0110	819	0110	873	1011	927	1011
658	1101	712	1101	766	1101	820	1101	874	0110	928	0110
659	1011	713	1010	767	1011	821	1011	875	1101	929	1101
660	0110	714	0101	768	0110	822	0110	876	1011	930	1011
661	1101	715	1011	769	1101	823	1101	877	0110	931	0110
662	1011	716	1011	770	1011	824	1011	878	1101	932	1101
663	0110	717	0110	771	0110	825	0110	879	1010	933	1011
664	1101	718	1101	772	1101	826	1101	880	0101	934	0110
665	1011	719	1011	773	1011	827	1011	881	1011	935	1101
666	0110	720	0110	774	0110	828	0110	882	0110	936	1011
667	1101	721	1101	775	1101	829	1101	883	1101	937	0110
668	1011	722	1011	776	1101	830	1011	884	1011	938	1101
669	0110	723	0110	777	1011	831	0110	885	0110	939	1011
670	1101	724	1101	778	0110	832	1101	886	1101	940	0110
671	1011	725	1011	779	1101	833	1011	887	1011	941	1101
672	0110	726	0110	780	1010	834	0110	888	0110	942	1011
673	1101	727	1101	781	0101	835	1101	889	1101	943	0110
674	1011	728	1011	782	1011	836	1101	890	1011	944	1101
675	0110	729	0110	783	0110	837	1011	891	0110	945	1010
676	1101	730	1101	784	1101	838	0110	892	1101	946	0101
677	1011	731	1011	785	1011	839	1101	893	1011	947	1011
678	0110	732	0110	786	0110	840	1011	894	0110	948	0110
679	1101	733	1101	787	1101	841	0110	895	1101	949	1101
680	1010	734	1011	788	1011	842	1101	896	1101	950	1011
681	0101	735	0110	789	0110	843	1011	897	1011	951	0110
682	1011	736	1101	790	1101	844	0110	898	0110	952	1101
683	0110	737	1011	791	1011	845	1101	899	1101	953	1011
684	1101	738	0110	792	0110	846	1010	900	1011	954	0110
685	1011	739	1101	793	1101	847	0101	901	0110	955	1101
686	1011	740	1011	794	1011	848	1011	902	1101	956	1101
687	0110	741	0110	795	0110	849	0110	903	1011	957	1011
688	1101	742	1101	796	1101	850	1101	904	0110	958	0110
689	1011	743	1011	797	1011	851	1011	905	1101	959	1101
690	0110	744	0110	798	0110	852	0110	906	1011	960	1011
691	1101	745	1101	799	1101	853	1101	907	0110	961	0110
692	1011	746	1101	800	1011	854	1011	908	1101	962	1101
693	0110	747	1010	801	0110	855	0110	909	1011	963	1011
694	1101	748	0101	802	1101	856	1101	910	0110	964	0110
695	1011	749	1011	803	1011	857	1011	911	1101	965	1101
696	0110	750	0110	804	0110	858	0110	912	1010	966	1011
697	1101	751	1101	805	1101	859	1101	913	0101	967	0110
698	1011	752	1011	806	1101	860	1011	914	1011	968	1101
699	0110	753	0110	807	1011	861	0110	915	0110	969	1011
700	1101	754	1101	808	0110	862	1101	916	1101	970	0110
701	1011	755	1011	809	1101	863	1011	917	1011	971	1101

TABLE 7-1. ASSYMETRIC SLANT PATTERN (CONT'D)

LOC	CONTENTS	LOC	CONTENTS
972	1011	998	1101
973	0110	999	1011
974	1101	1000	0110
975	1011	1001	1101
976	0110	1002	1011
977	1101	1003	0110
978	1010	1004	1101
979	0101	1005	1011
980	1011	1006	0110
981	0110	1007	1101
982	1101	1008	1011
983	1011	1009	0110
984	0110	1010	1101
985	1101	1011	1010
986	1101	1012	0101
987	1011	1013	1011
988	0110	1014	0110
989	1101	1015	1101
990	1011	1016	1101
991	0110	1017	1011
992	1101	1018	0110
993	1011	1019	1101
994	0110	1020	1011
995	1101	1021	0110
996	1011	1022	1101
997	0110	1023	1011?

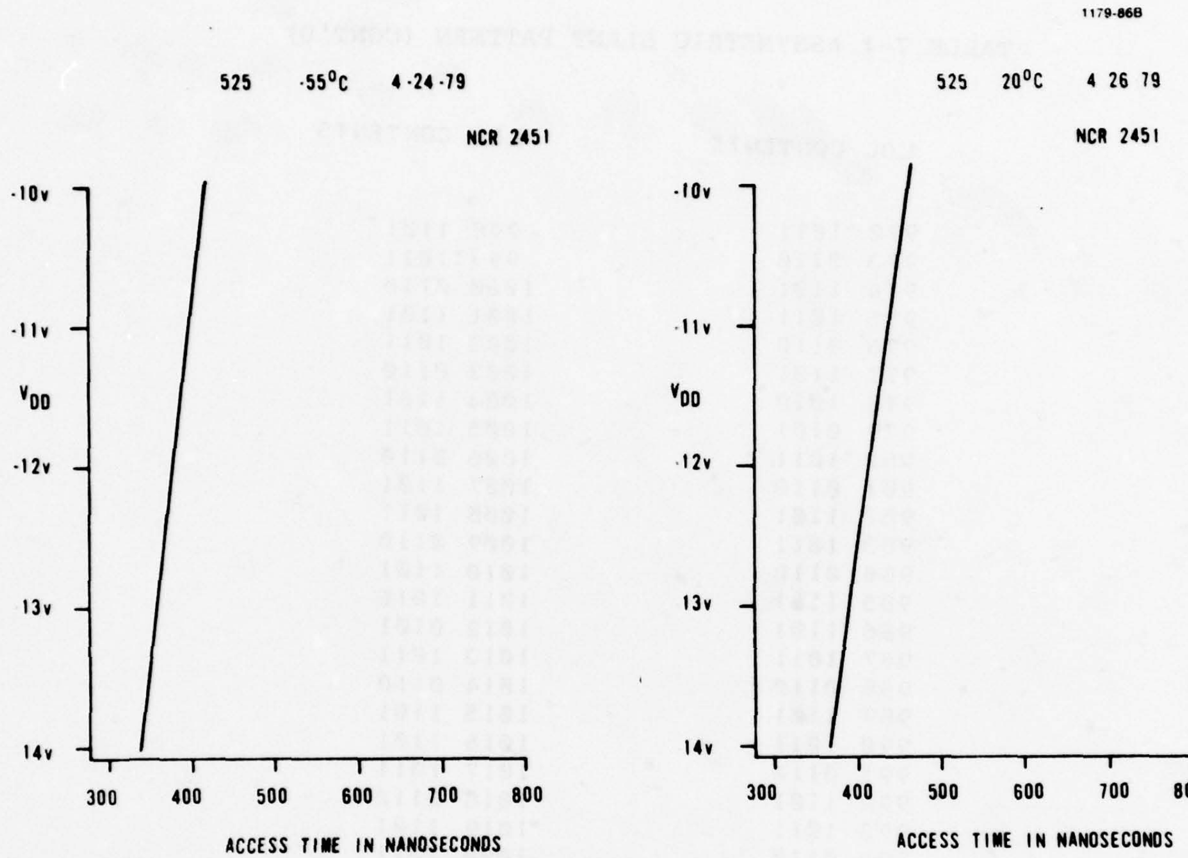


FIGURE 7-2. ACCESS TIME CHARACTERISTIC OF NCR 2451

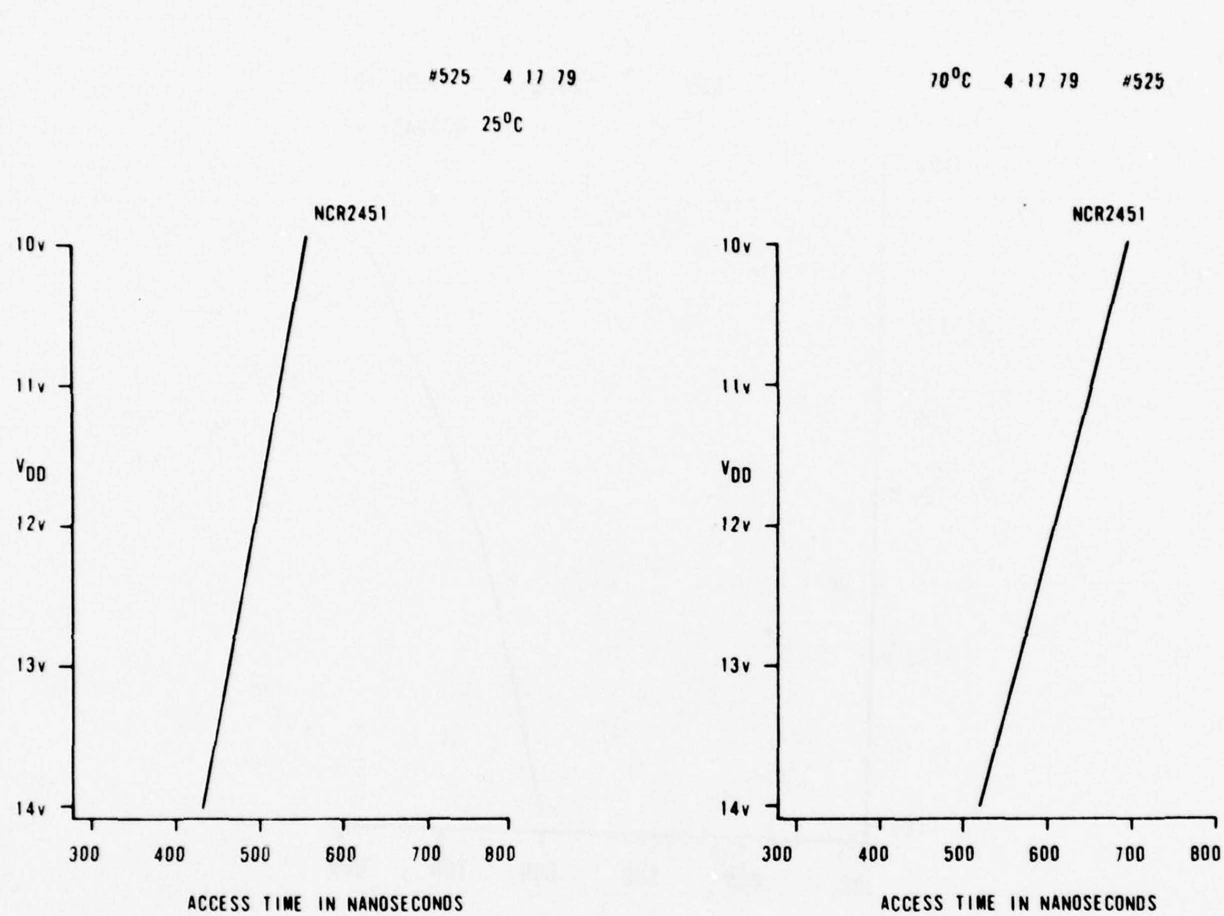


FIGURE 7-2. ACCESS TIME CHARACTERISTIC OF NCR 2451 (Cont)

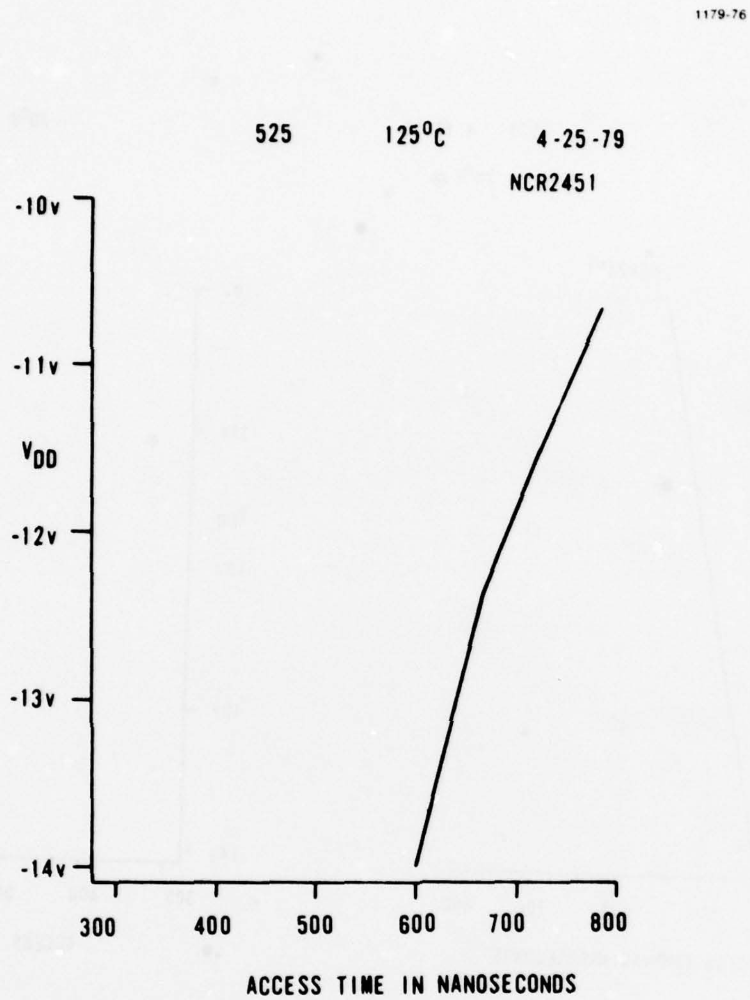


FIGURE 7-2. ACCESS TIME CHARACTERISTIC OF NCR 2451 (Cont)

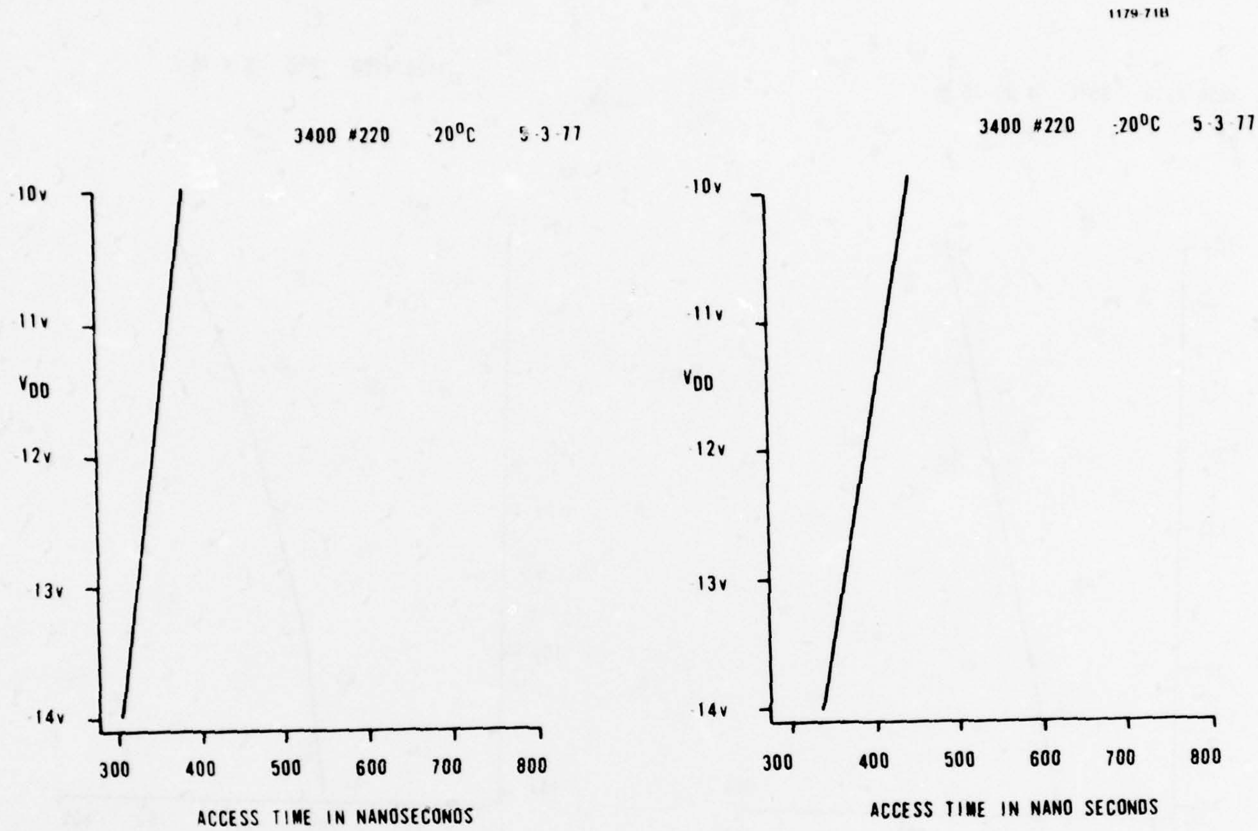


FIGURE 7-3. ACCESS TIME CHARACTERISTIC OF GI ER3400

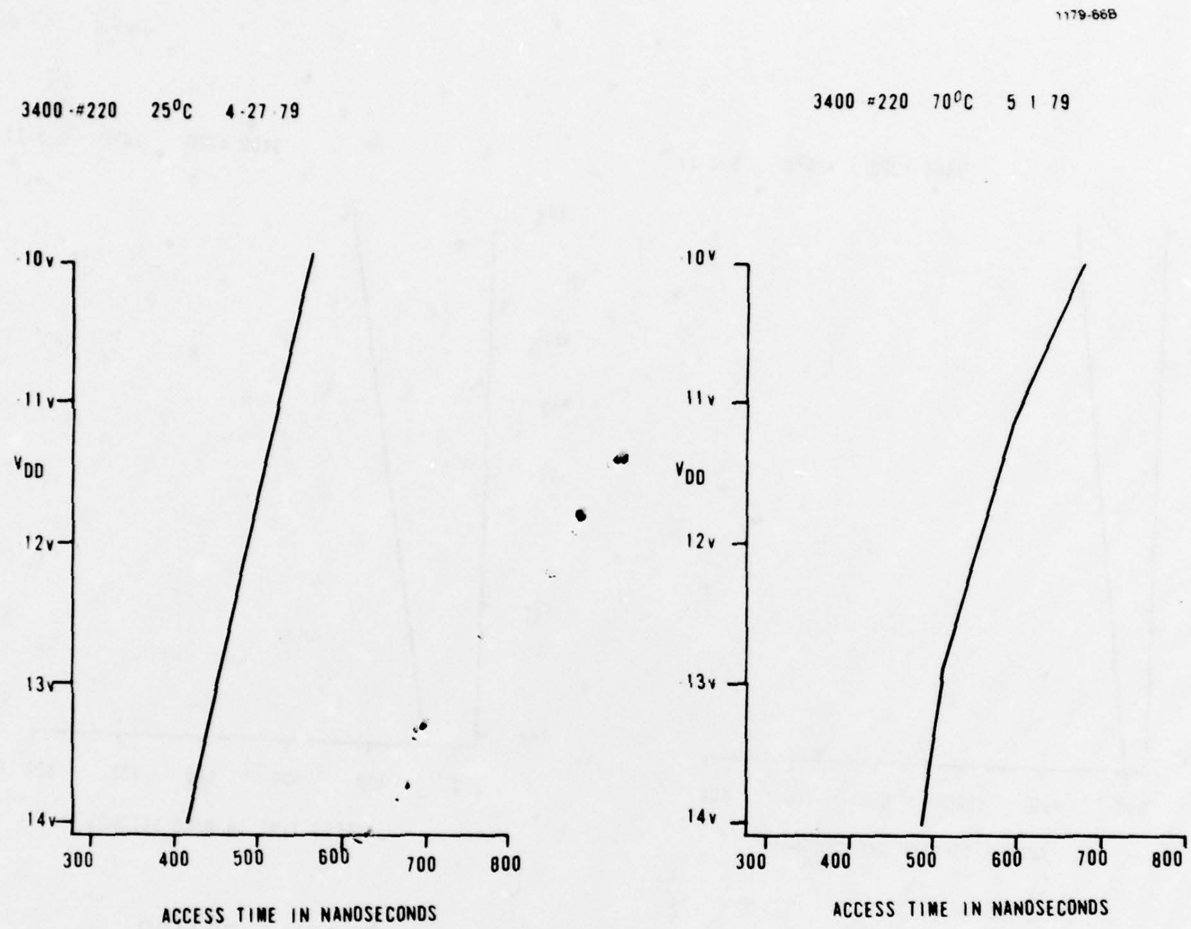


FIGURE 7-3. ACCESS TIME CHARACTERISTIC OF GI ER3400 (Cont)

1179-235

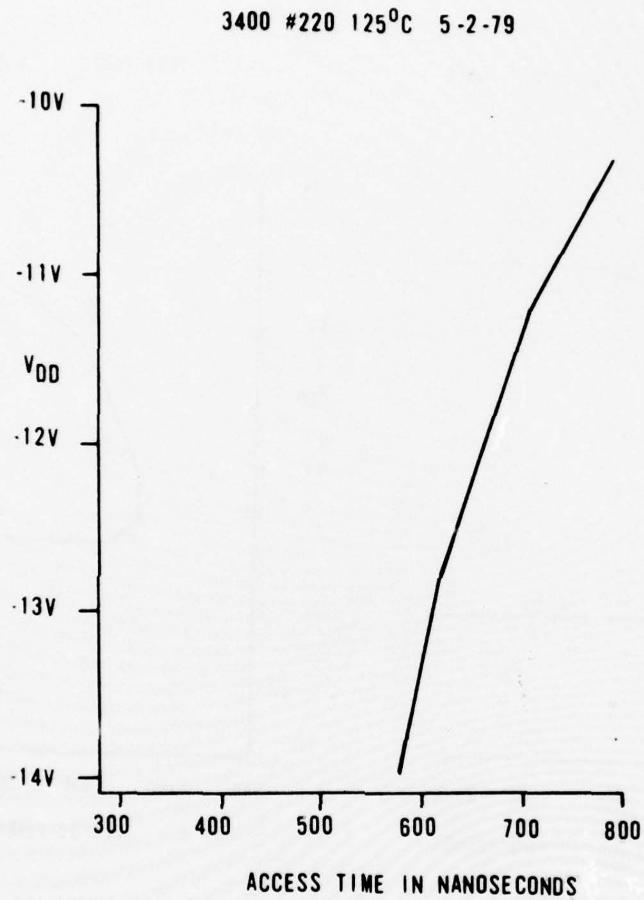


FIGURE 7-3. ACCESS TIME CHARACTERISTIC OF GI ER3400 (Cont)

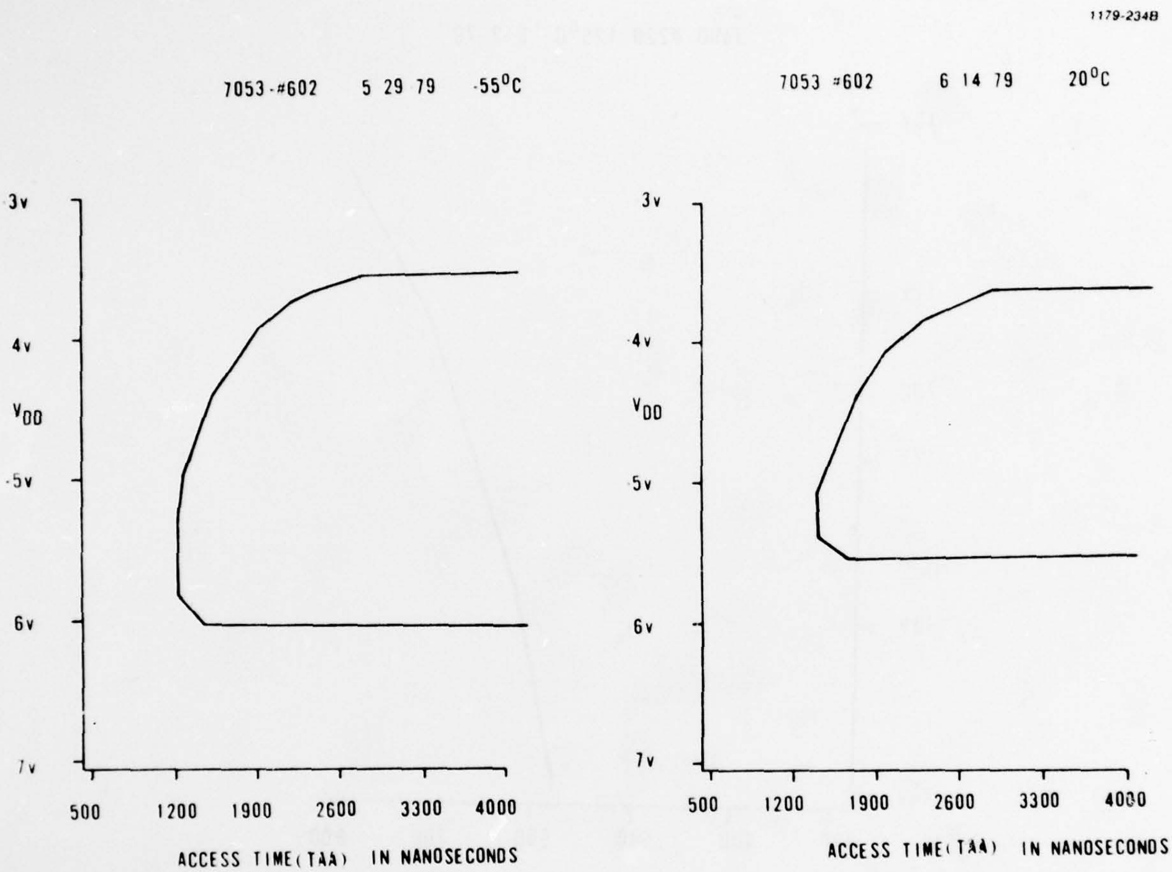


FIGURE 7-4. ACCESS IN CHARACTERISTIC OF NITRON NC7053

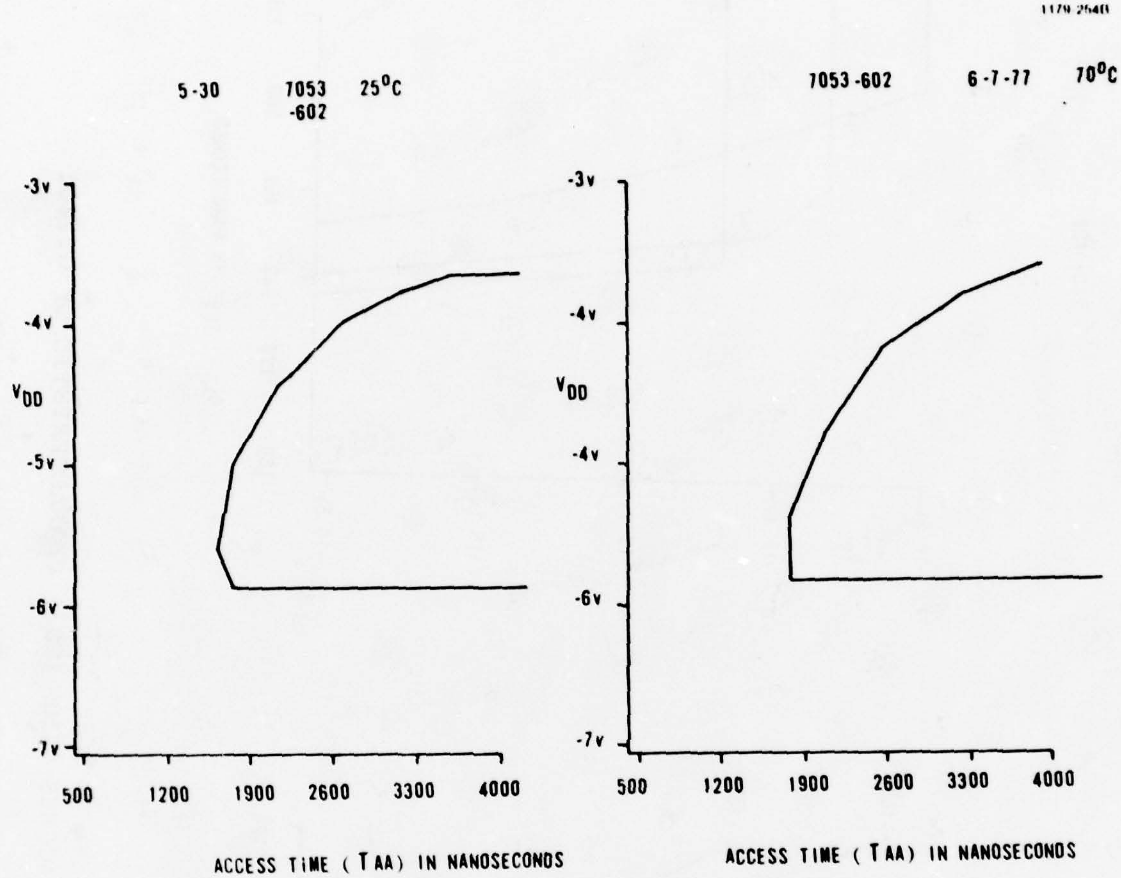


FIGURE 7-4. ACCESS IN CHARACTERISTIC OF NITRON NC7053 (Cont)

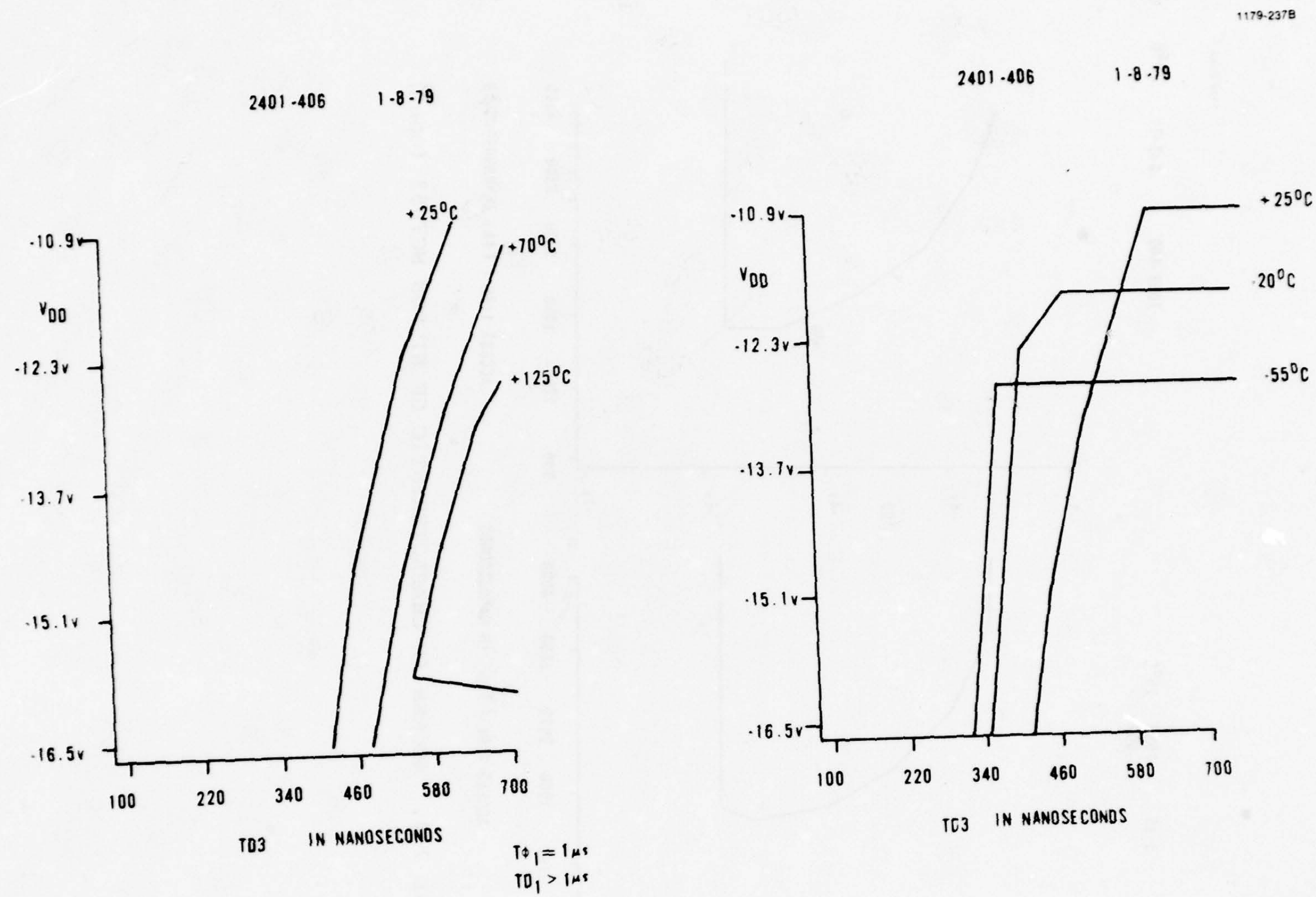


FIGURE 7-5. ACCESS TIME (TD3) CHARACTERISTIC OF GT2401

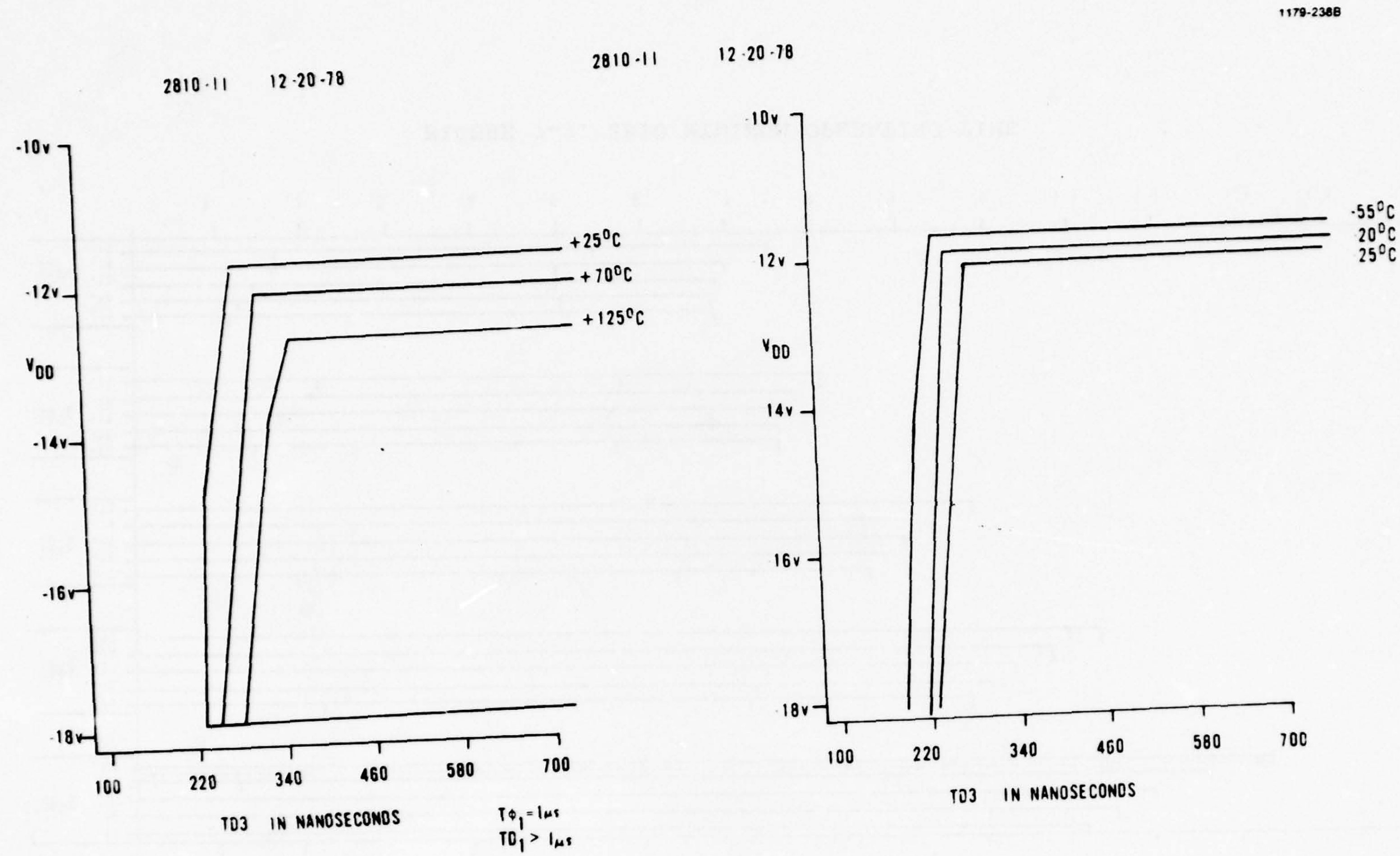


FIGURE 7-6. ACCESS TIME (TD3) CHARACTERISTIC OF NCR 2810

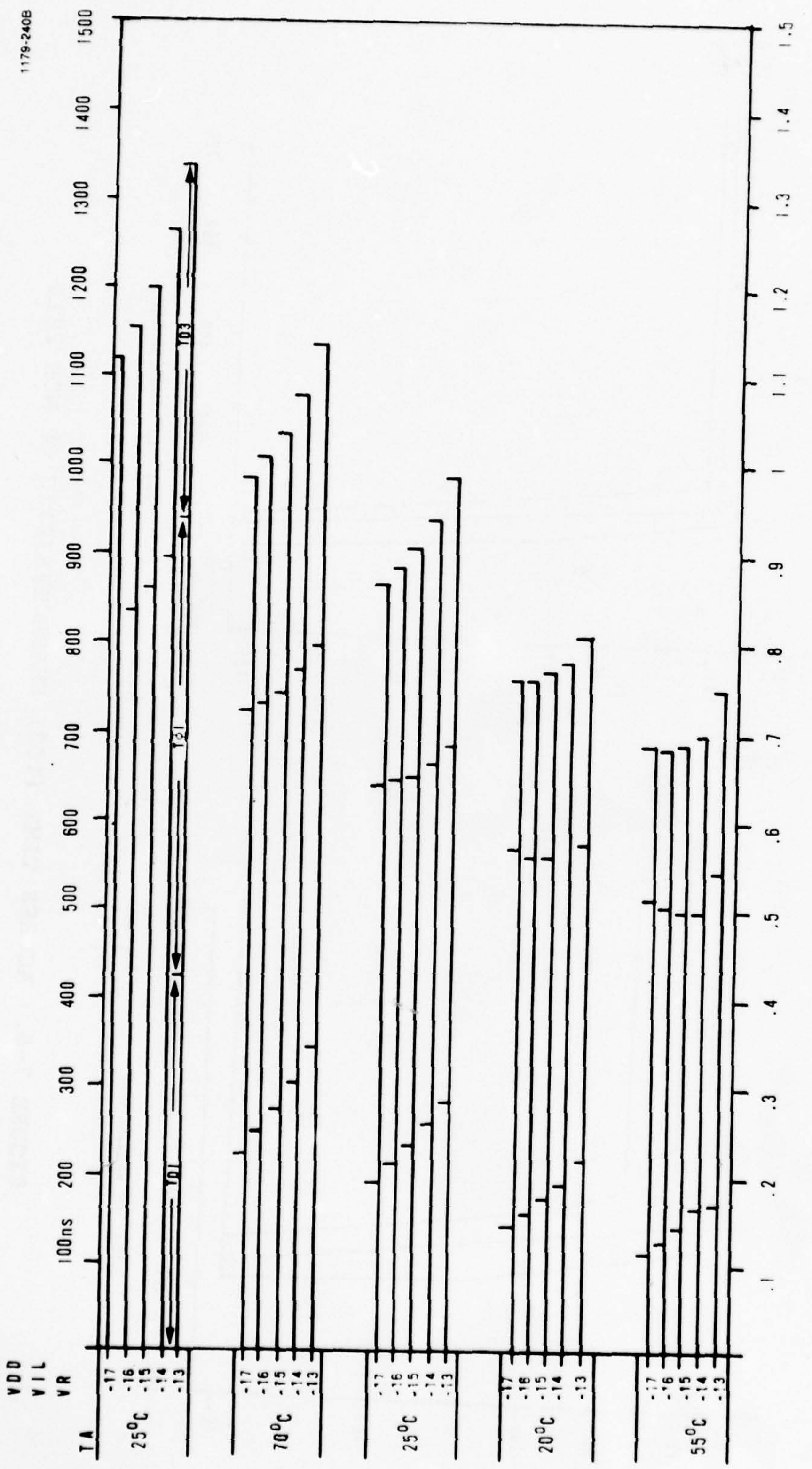


FIGURE 7-7. 2810 MINIMUM OPERATING TIME

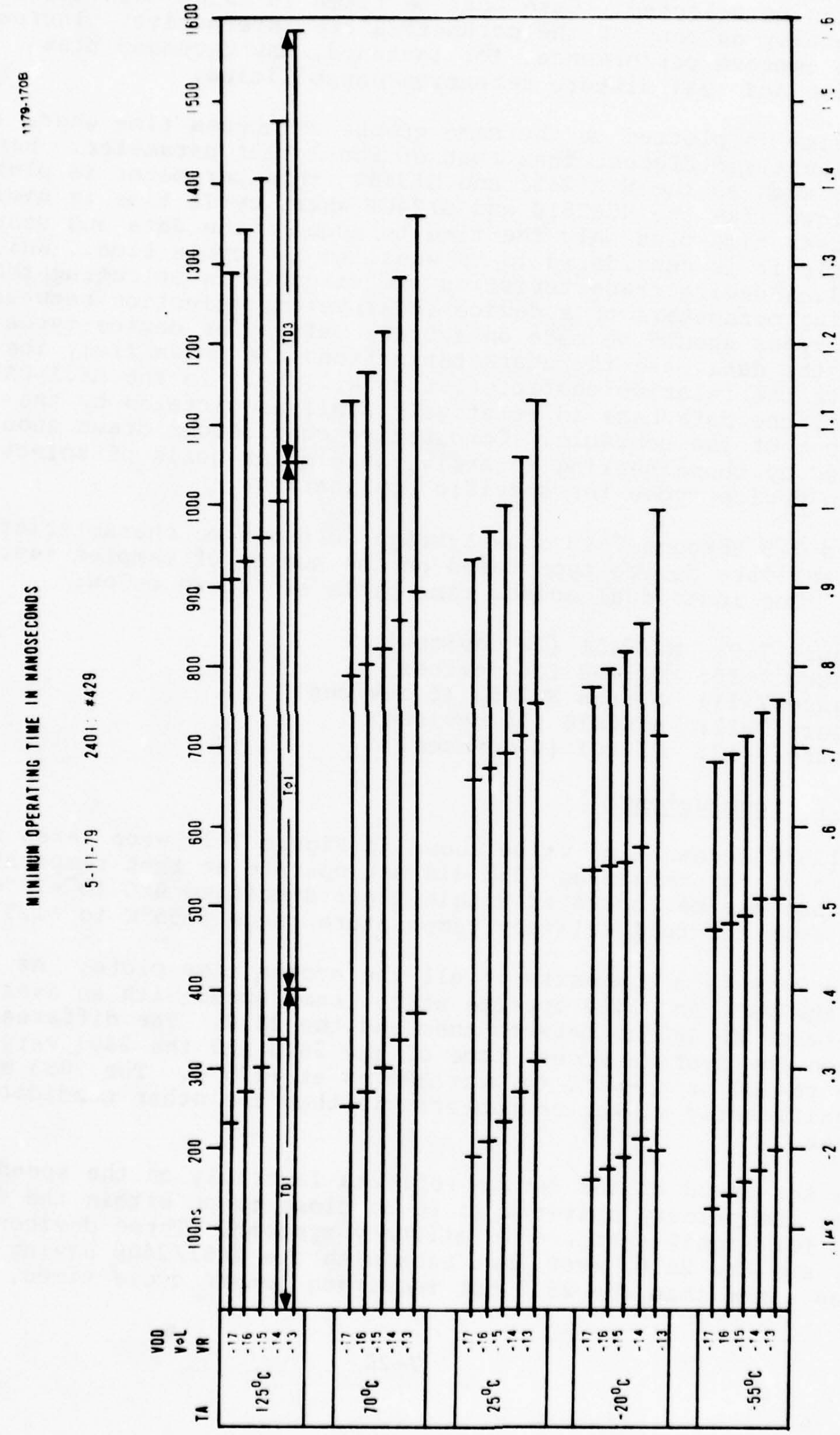


FIGURE 7-8. MINIMUM OPERATING TIME IN NANOSECONDS

range can be selected. Care must be taken in using this data unilaterally as many of the parameters are interactive. Increasing bias to improve performance, for instance, may decrease bias retention and read disturb retention capabilities.

Cycle time is plotted on the same graphs as access time where it is significantly different than that of the latter parameter. Hence for devices such as the NCR 2451 and GI3400, this parameter is plotted. In devices like the NCR2810 and GI2401 where cycle time is similar to the access time plus only the time to acquire the data and start the new cycle it is considered to be equal to the cycle time. While individual device characteristics are valuable in selecting the operating parameters of a device in a system, selection between device types should be made on average values for device types. The larger the data base the characterizations are drawn from, the more accurate the relative characteristics will be. In the MACI-EAROM Program, the data base is relatively small as dictated by the time and scope of the schedule. Comparative conclusions drawn should be verified by those seeking to arrive at similar goals of selecting optimum device types for specific applications.

Figures 7-9 through 7-13 show average access time characteristics for each candidate device type based on the number of samples tested as shown. The individual access time plots are shown below:

Figure 7-9: NCR2451 (10 devices)
Figure 7-10: GI3400 (10 devices)
Figure 7-11: Nitron NC7053 (5 devices)
Figure 7-12: NCR2810 (10 devices)
Figure 7-13: GI2401 (4 devices)

7.1.1.4 Conclusions

The +125°C access time value shown in Figure 7-11 were taken from two devices as the remaining 7053 did not operate at that temperature. All other devices operated within their specified 0°C to +70°C access times over the full military temperature range (-55°C to +125°C).

Figure 7-14 is a composite of all the access time plots. As can be seen the 2451 and 3400 operate at the same speed with an average difference of 400 ns between them and the 2810. The difference between the average access time of the 2810 and the 2401 vary from close to 100 ns a -55°C to over 300 ns at +125°C. The 7053 exhibits a significantly slower characteristic than the other candidate devices.

While the speed of the device reflects favorably on the speedier parts, the primary criteria is to be close to or within the desired range for significant use in military systems. Three devices: 2451, 3400, and the 2810, meet that test with the 2451/3400 having faster access times than the 2810 but requiring longer cycle times.

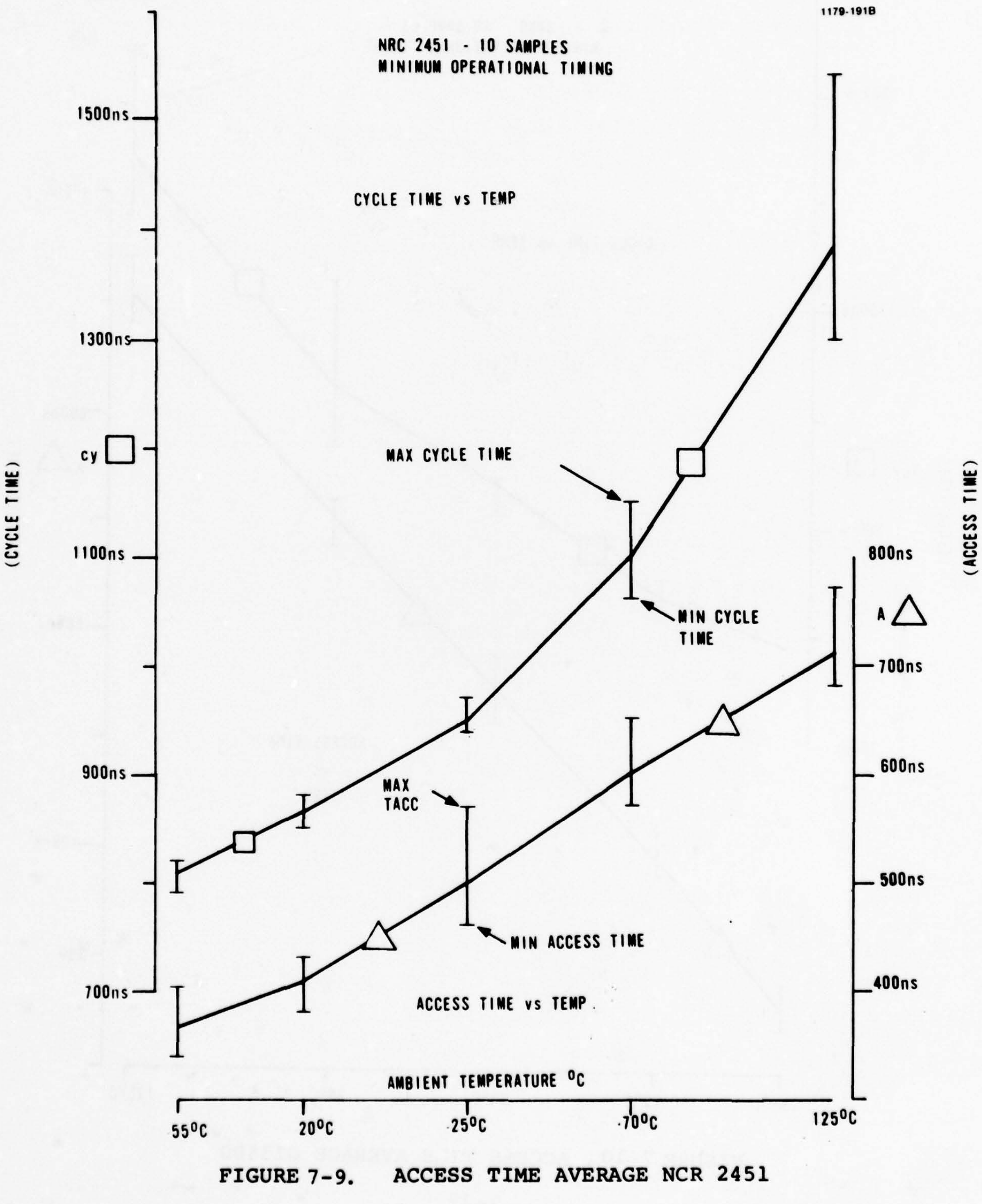


FIGURE 7-9. ACCESS TIME AVERAGE NCR 2451

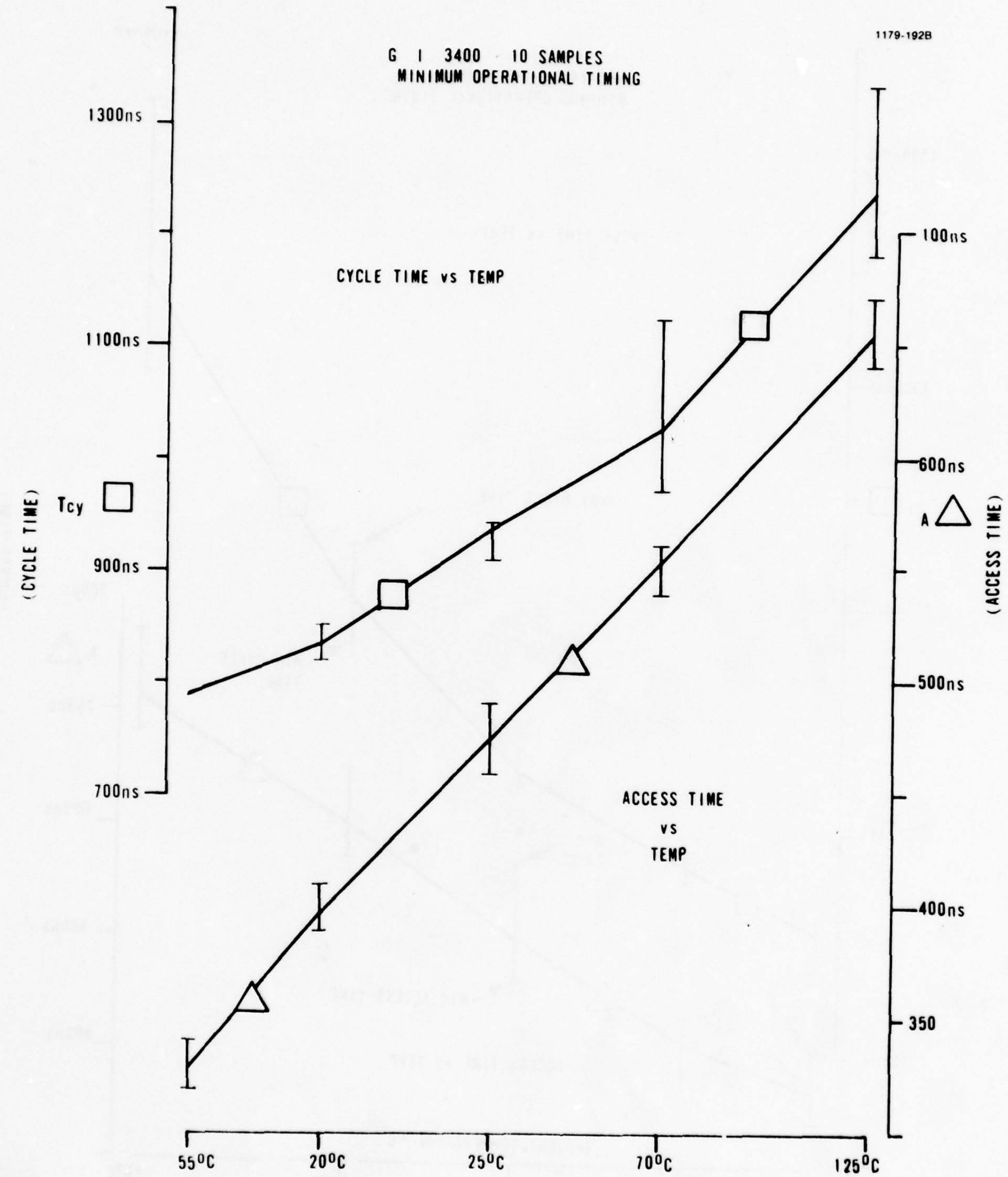


FIGURE 7-10 . ACCESS TIME AVERAGE GI3400

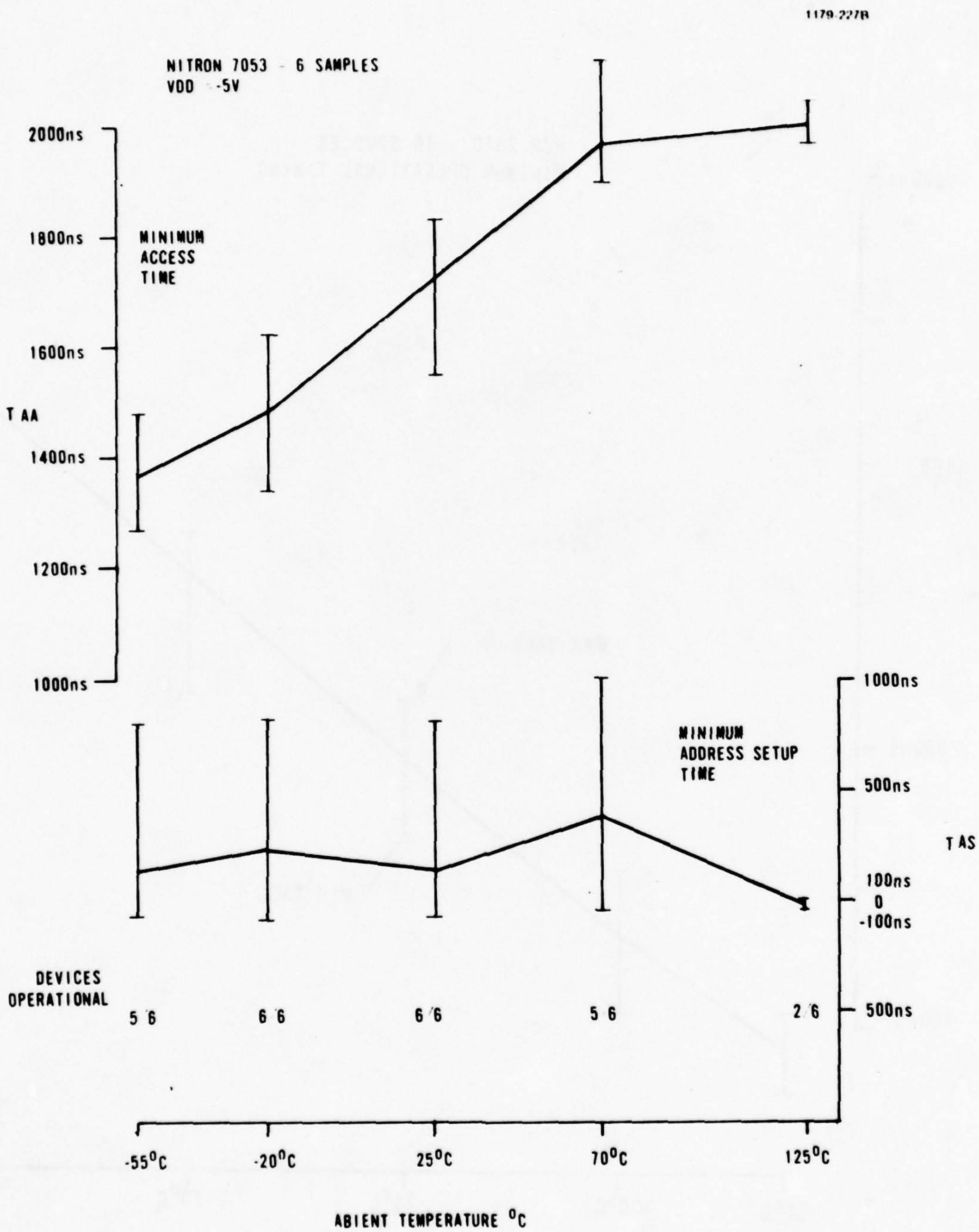


FIGURE 7-11 . AVERAGE ACCESS TIME NITRON 7053

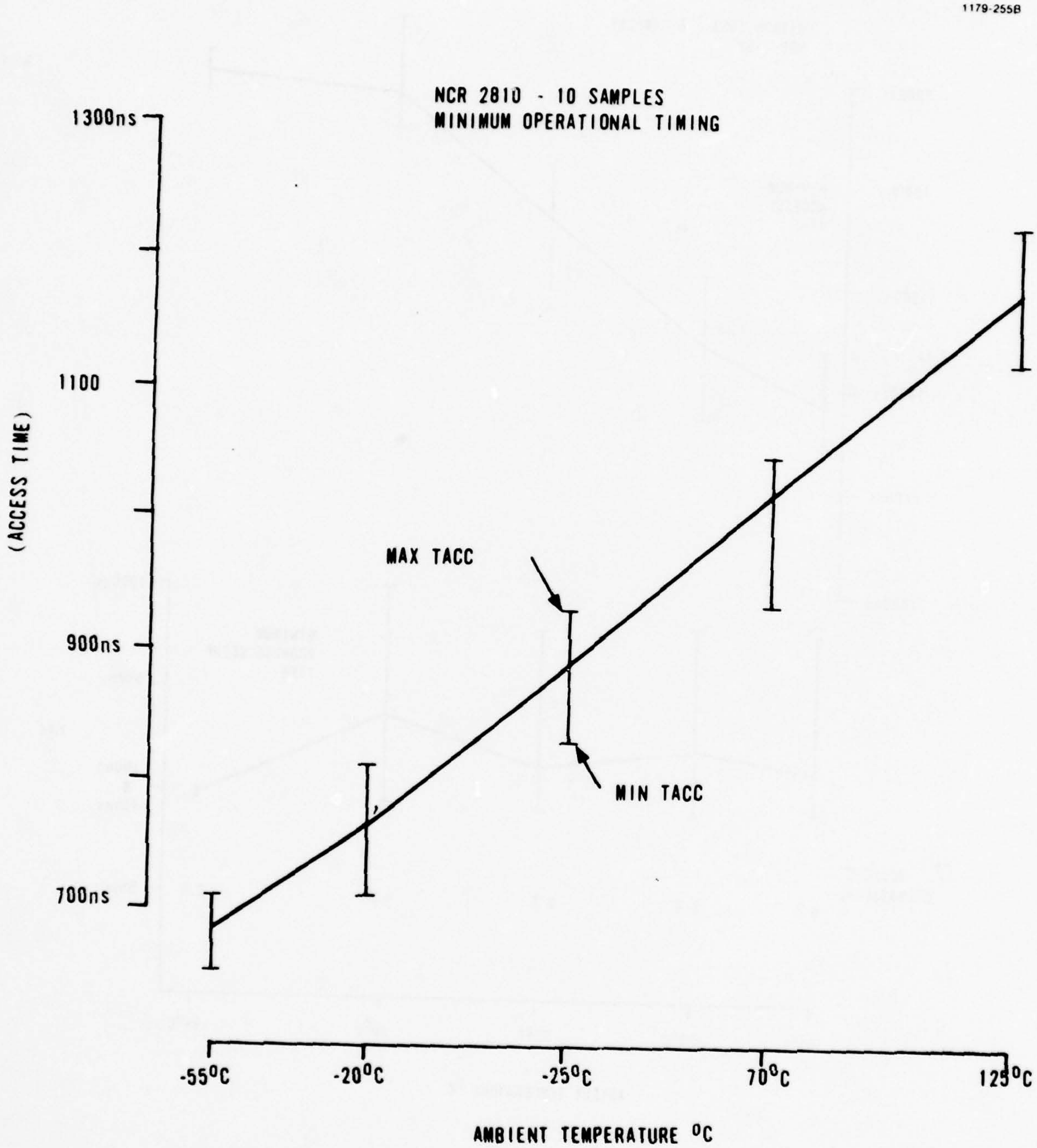


FIGURE 7-12. AVERAGE ACCESS TIME NCR 2810

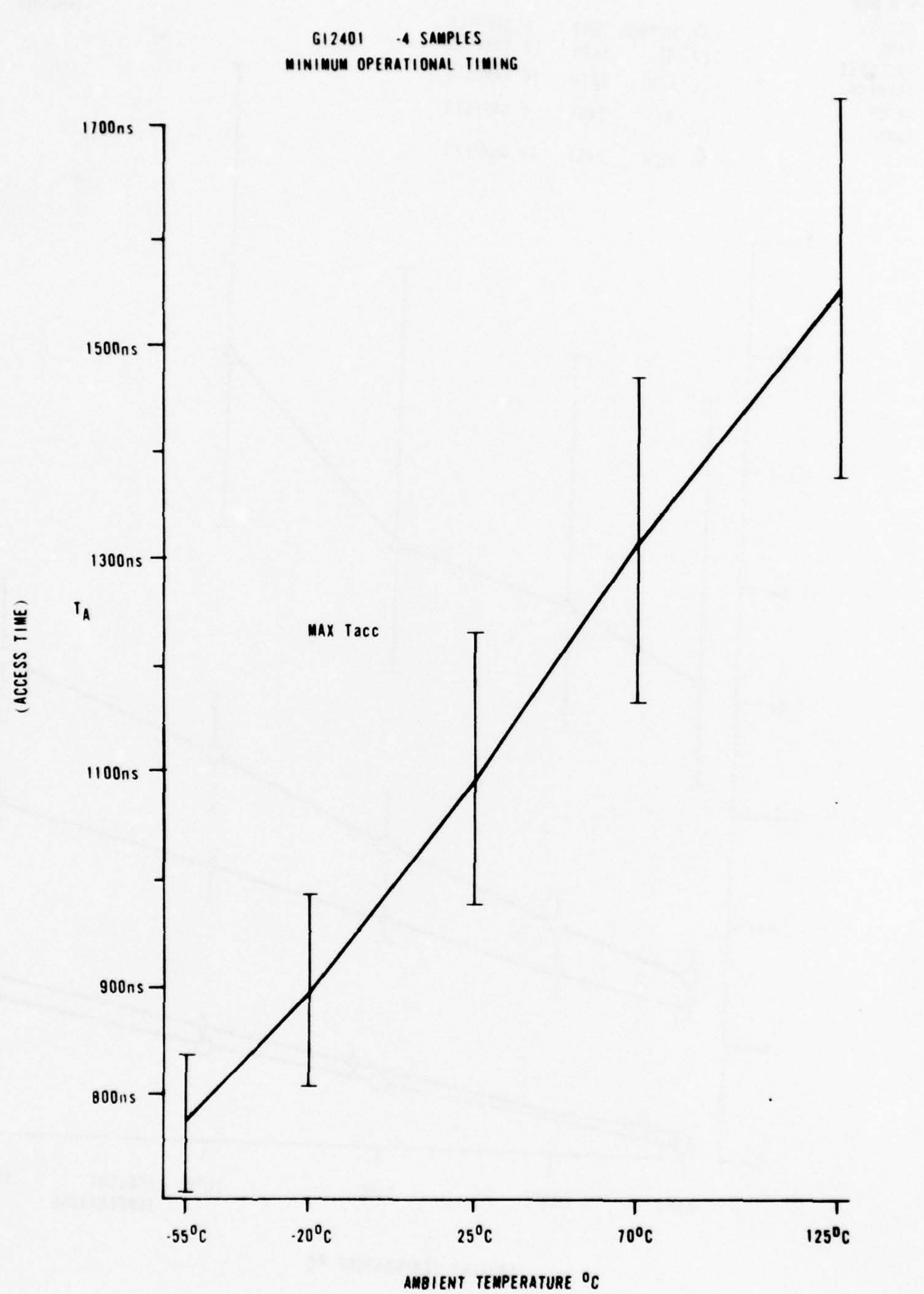


FIGURE 7-13. AVERAGE ACCESS TIME GI2401

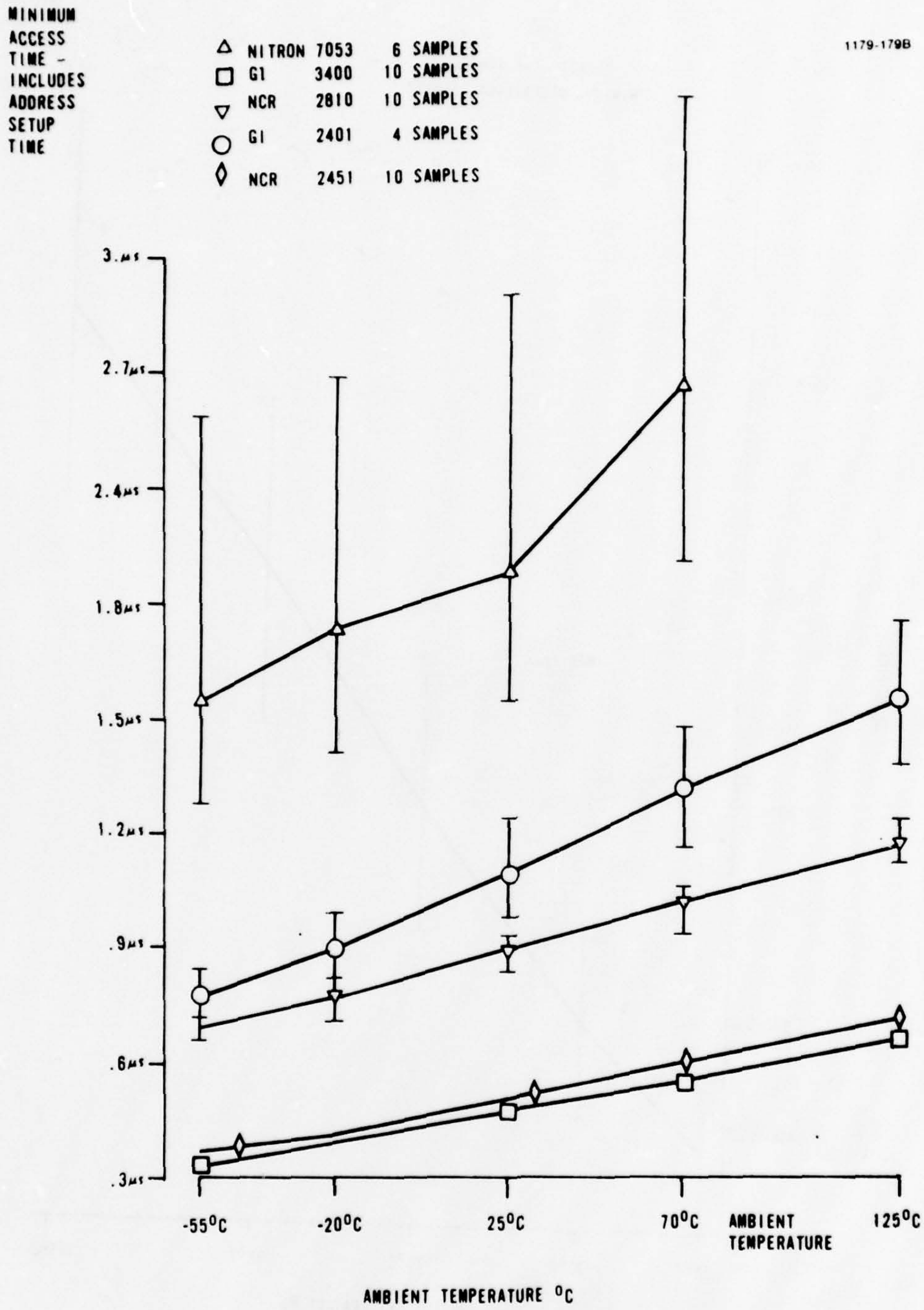


FIGURE 7-14. ACCESS TIMES COMPOSITE

Another way of measuring whether a device is suitable for application to military use is to show the yield of devices to a desired specification over the desired range. Figure 7-15 plots the yield of NCR 2451 to 900ns, 600ns, and 400ns at different bias conditions. It shows the temperature range over which that yield of devices will operate.

The first row shows that 100 percent of the 2451's tested will operate within the manufacturer's specified value of access time (specified for 0°C to +70°C) over the full military range at the nominal bias specified on the data sheet. The schmoo plots of Figure 7-2 show the 2451 plotted approaches the specified value only at +125°C with an applied bias of less than the specified range of -12V ±0.6vdc. By combining this data it can be seen that a wide margin of operation exists for full military range operation of the 2451 for this parameter. The remaining data in this table shows potential yield using these devices to faster access times and increased bias.

7.1.2 Cycle Time

This parameter is defined as being the minimum time between address input changes on successive minimum memory cycles and is illustrated in Figure 7-1 for both clocked and nonclocked cycles. This parameter is important as a distinct measurement only when it differs significantly from the access time measurement.

It was found that in the devices using the clocked cycles (i.e., NCR 2810 and GI2401) the cycle time was similar to the access time with a 50 to 100ns offset to allow acquiring of the data. For this reason the data in Figures 7-5 through 7-8 applies equally to cycle time.

7.1.2.1 Results

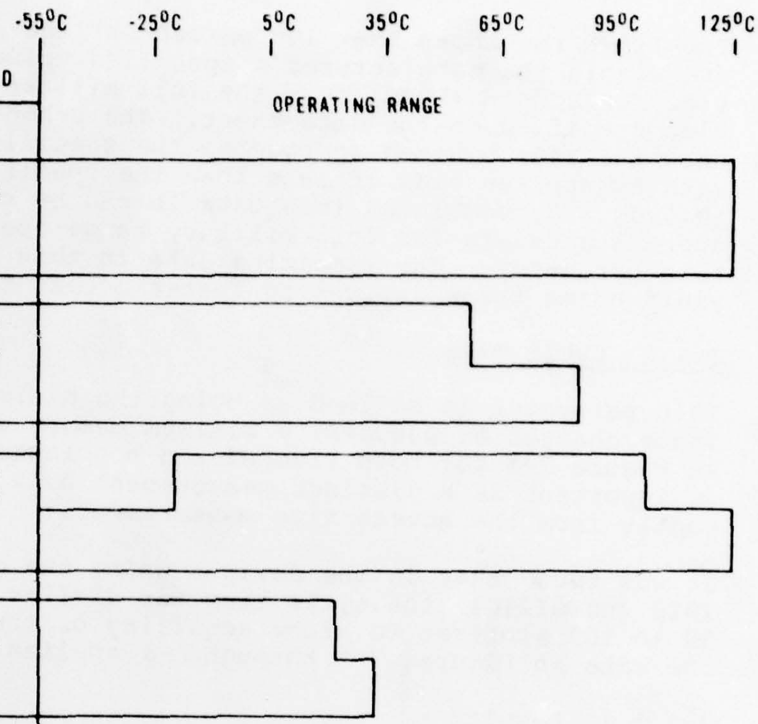
In the cases of the nonclocked cycle devices (i.e., 2451, 3400, and 7053), schmoos were plotted showing the relationship between chip enable "on" time, varied bias conditions and the cycle time. Plots were made at selected ambient temperature to determine the effects over military range values. Figures 7-16 and 7-17 show the variation of this parameter over bias and temperature in these two devices. The difference between the "chip enable" on time and the cycle time represents the "recovery time" required by the device before a new cycle can be initiated.

7.1.2.2 Conclusions

In applications where repeated hits upon memory are at the fastest rate possible, such as in secondary memory dumping into primary memory or computer operations not having execute and fetch cycles, cycle time becomes a limiting factor. It should, therefore, be compared to access time of other memory types having similar access

1179-106B

DEVICE	SAMPLE SIZE	VDD REFERENCE SUBSTRATE	ACCESS TIME	YIELD
2451	5	-17v*	900ns*	100%
2451	5	-17v*	600ns	100% 60%
2451	5	-19v	600ns	100% 60%
2451	5	-17v*	400ns	100% 80%



* AS SPECIFIED BY THE MANUFACTURER

** THIS DOES NOT INCLUDE SET UP (TD_1) AND CLOCK ($T_{\phi 1}$) TIME. IT IS SPECIFIED BY THE MANUFACTURER AS D3

FIGURE 7-15. YIELD OF TESTED DEVICES TO ACCESS TIME SPECIFICATION FOR NCR 2451

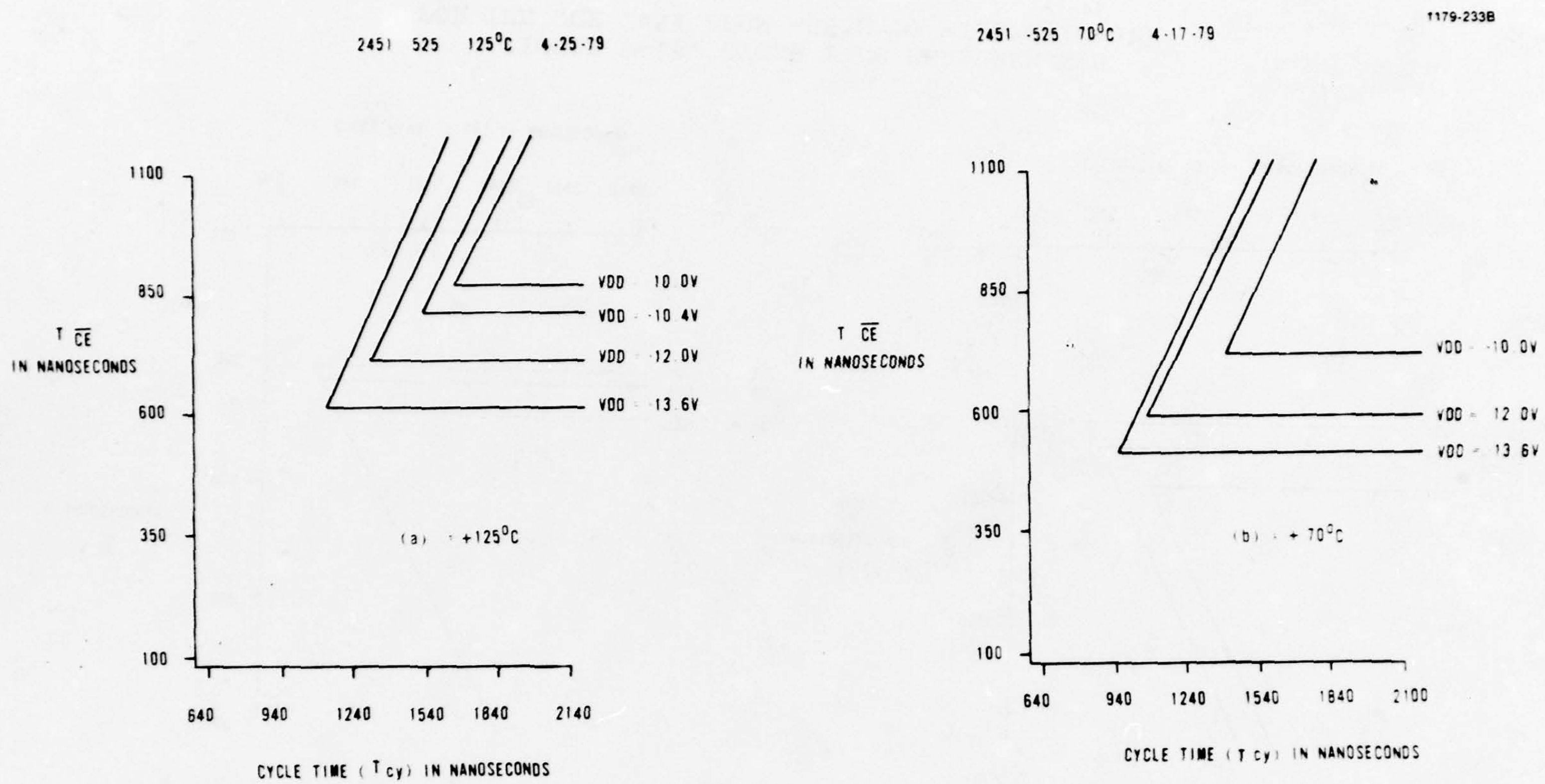


FIGURE 7-16. CYCLE TIME MEASUREMENTS
FOR THE NCR 2451 FROM -55°C TO +125°C

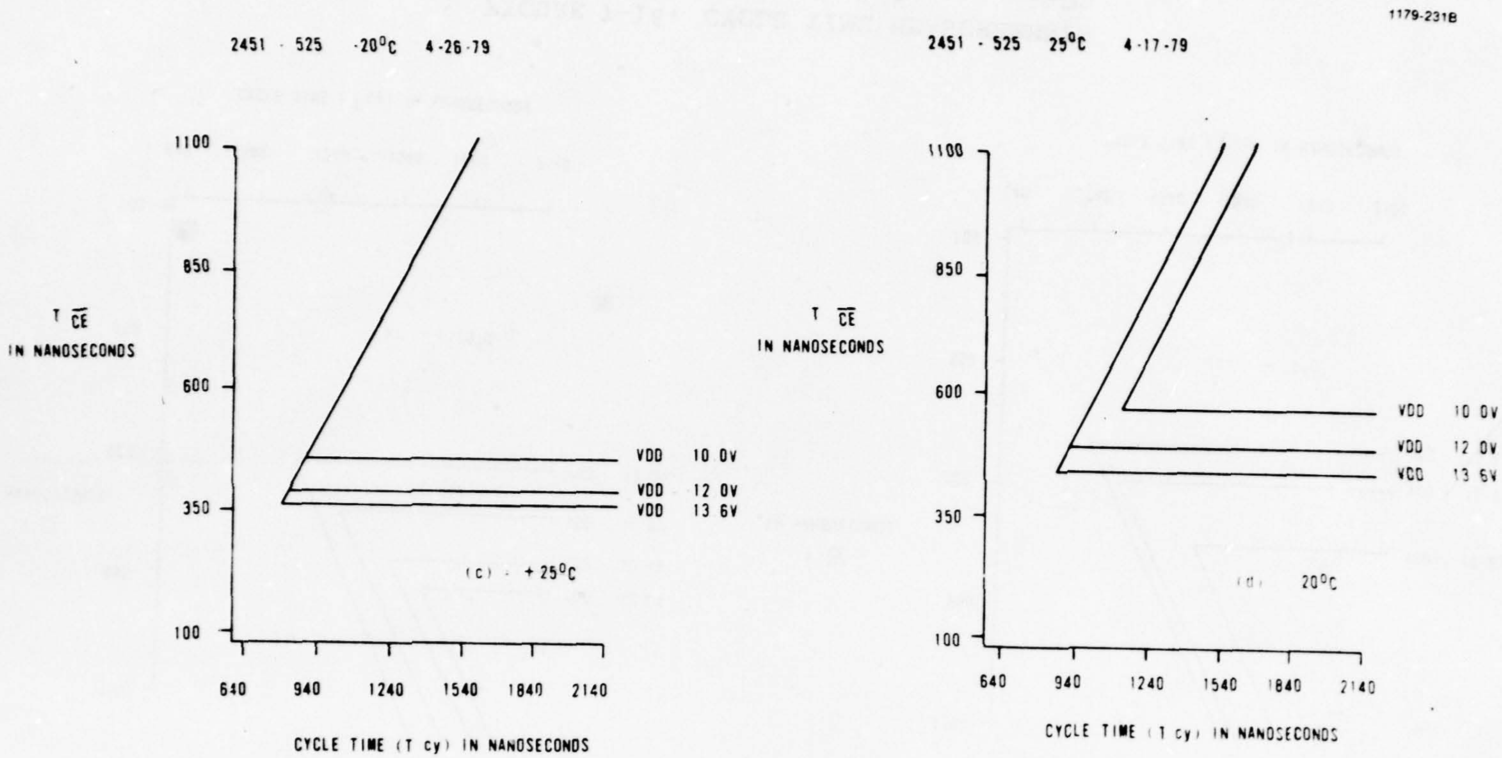
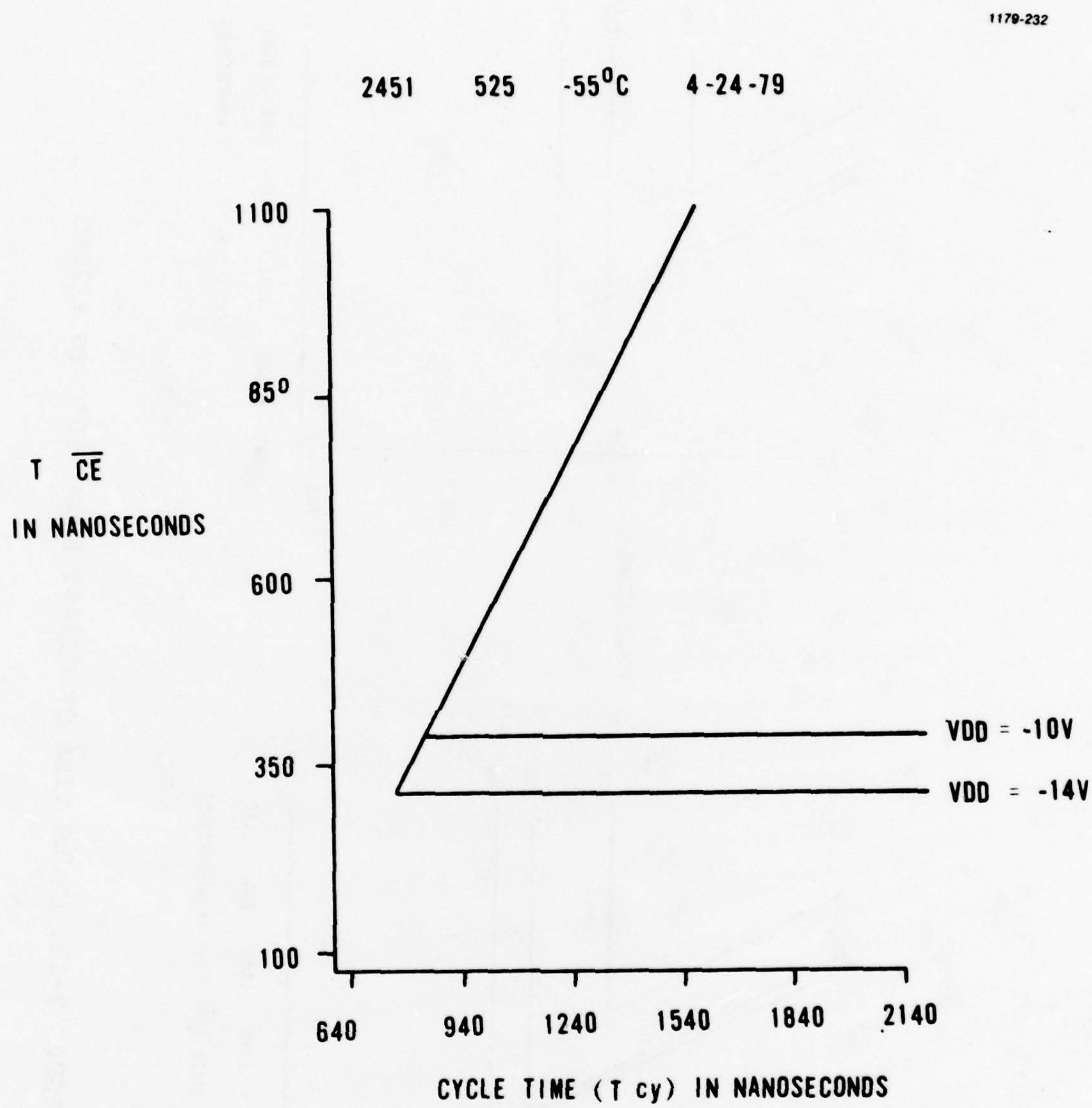
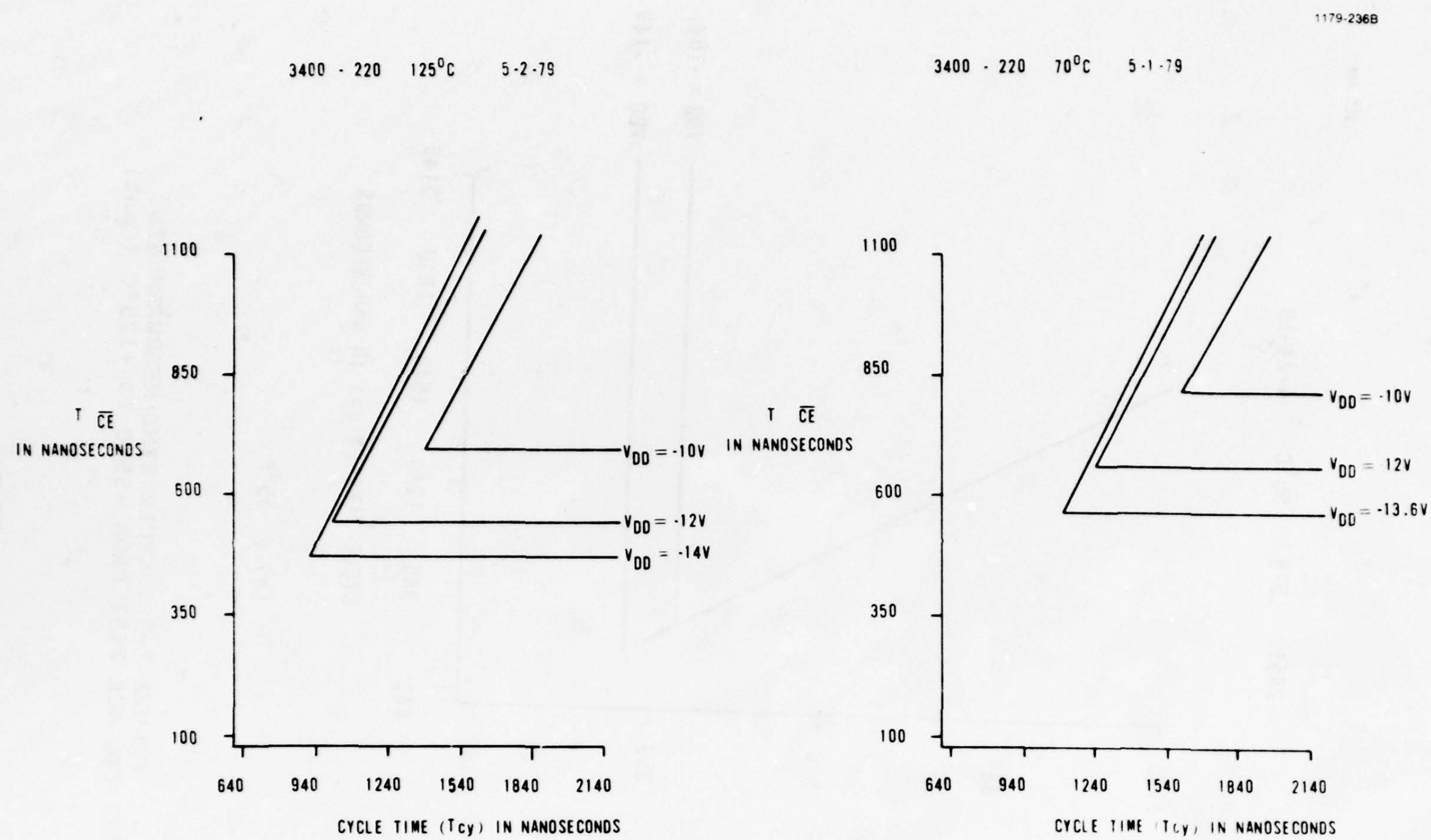


FIGURE 7-16. CYCLE TIME MEASUREMENTS
FOR THE NCR 2451 FROM -55°C TO +125°C (Cont)



(e) @ -55°C

FIGURE 7-16. CYCLE TIME MEASUREMENTS
FOR THE NCR 2451 FROM -55°C TO +125°C (Cont)



(b) - +70°C

(a) - +125°C

FIGURE 7-17. CYCLE TIME OF GI3400 FROM -55°C TO +125°C

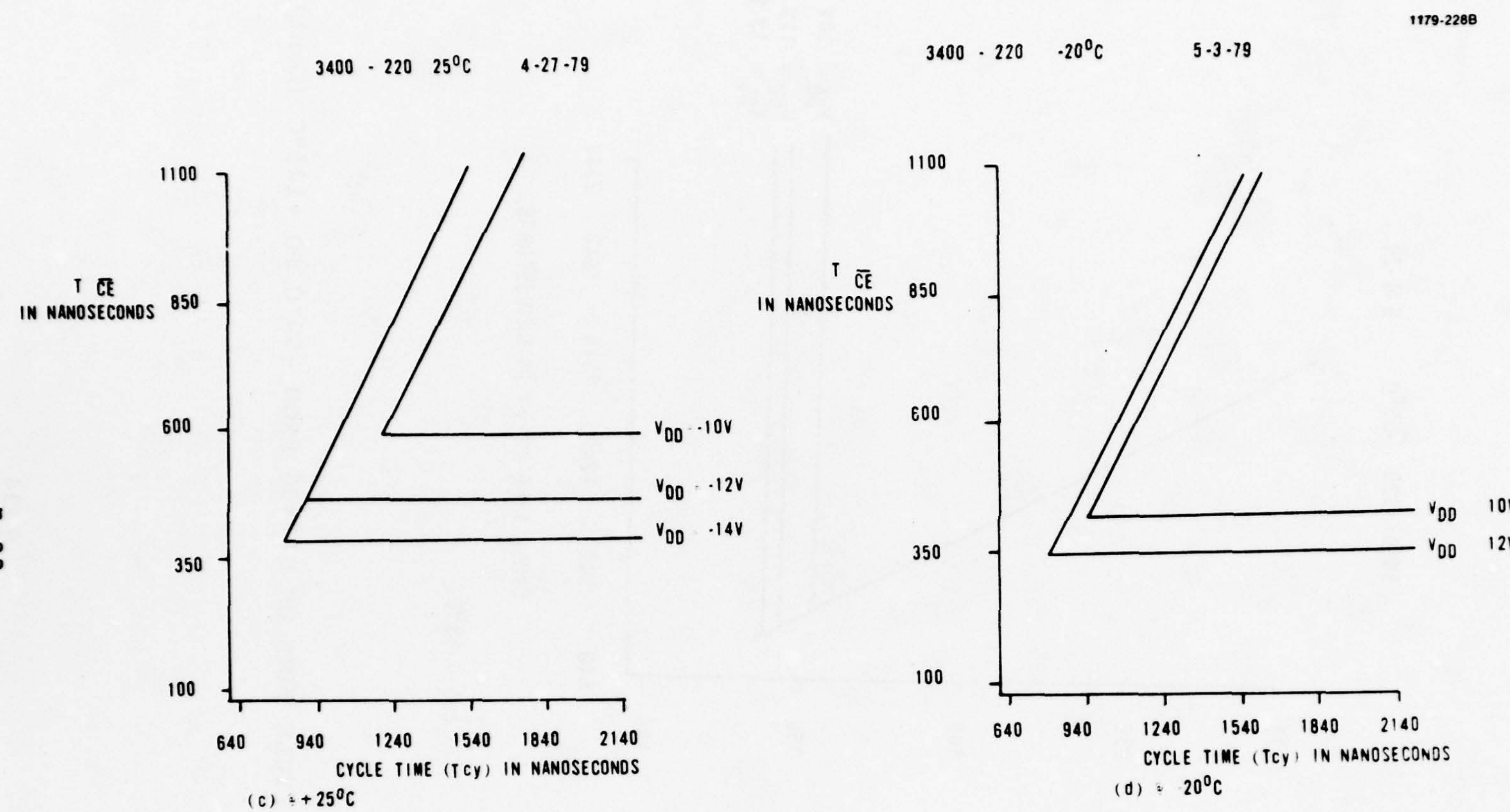
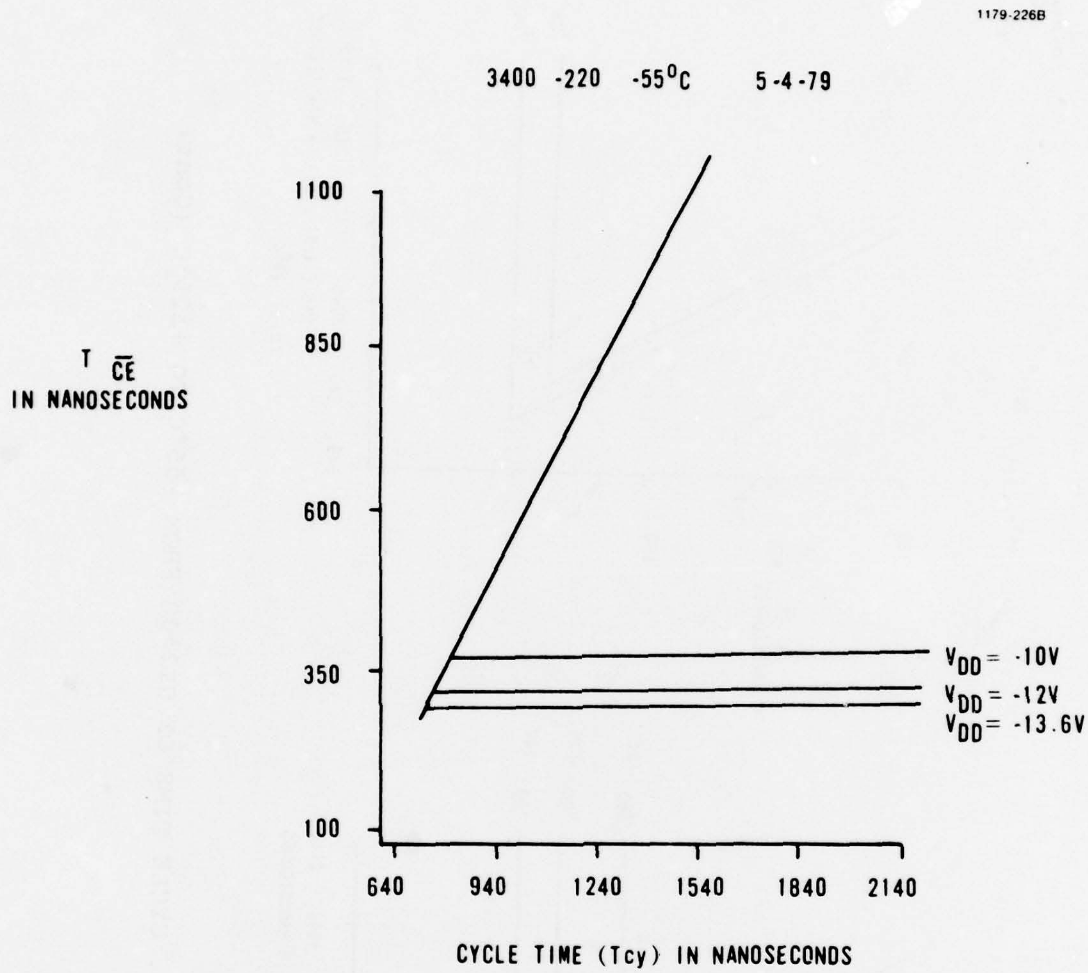


FIGURE 7-17. CYCLE TIME OF GI3400 FROM -55°C TO +125°C (Cont)



(e) @-55°C

FIGURE 7-17. CYCLE TIME OF GI3400 FROM -55°C TO +125°C (Cont)

and cycle times. Where execute and fetch cycles are distinctive (i.e., in some microprocessor operations like 6800, etc.) the recovery time may be transparent to the requirement. This is true because recovery can be timed to overlap the execute portion of the processor cycle. The importance of this parameter is, therefore, considered application dependent.

7.1.3 Power Supply Current

7.1.3.1 Significance of Parameter

The Military Applications Survey indicated that the power dissipation of the MNOS memory devices was an important criteria for their use. This parameter was considered a dynamic one since measurements were made with the devices operating in different modes. Pictures of current waveshapes were taken to show current spiking and peak values, to indicate decoupling and peak power supply current values required.

7.1.3.2 Results

Figures 7-18 through Figure 7-21 show the average power supply current for each supply of each device in all modes where significant current was detected. The most interesting results are that the 2451 and 3400 require more current in the read mode than either other active modes (i.e., write and erase). While the 2810 shows more current than the 2451/3400 devices in the write mode the position is reversed for the read mode. Considering current per bit of memory, the best device is the 2810 (0.00104/ma/bit) at +25°C and 0.0034 ma/bit at -55°C while the 2401 uses 0.00185 ma/bit at +25°C. Figures 7-22 through 7-25 show the current waveshapes for all modes at -55°C +25°C and +125°C for each candidate device.

7.1.3.3 Conclusions

The best device from a current per bit measurement appears to be the 2810 with a average current of 0.001 ma/bit in the active, operating read mode at +25°C. All devices require significant decoupling as can be seen from the waveshapes particularly at the clock and chip enable edges.

7.1.4 Radiation Resistance

While this parameter was not considered significant by most persons surveyed, in special applications it is critical. No attempt was made here to perform detailed radiation analysis or perform extensive testing. Using our in-house Flash X-ray facility, primarily used for dose rate testing, some data retention tests were performed to get a comparative look at the respective devices in this environment.

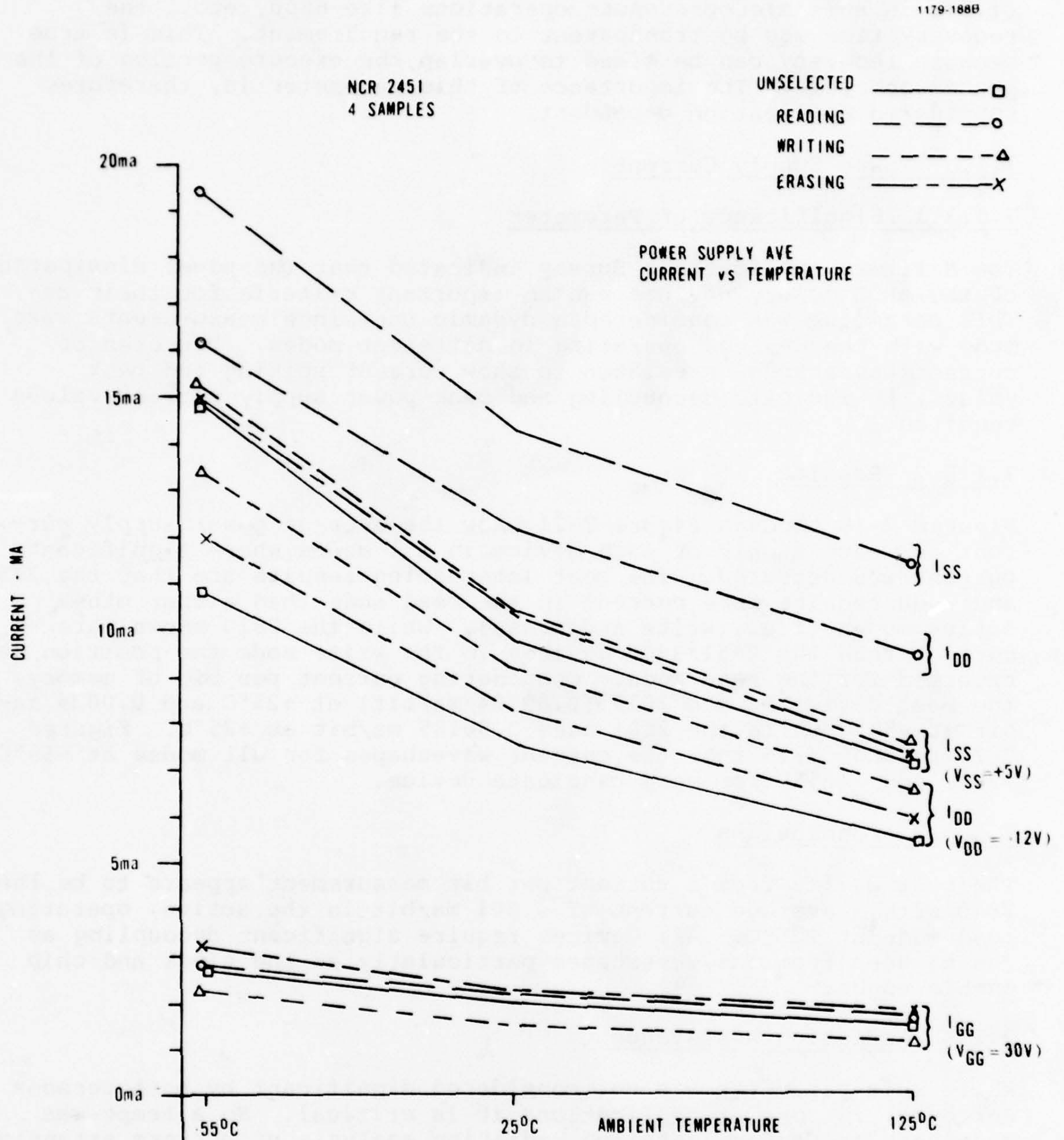


FIGURE 7-18. AVERAGE POWER SUPPLY CURRENT VS TEMPERATURE (AMBIENT) FOR NCR 2451

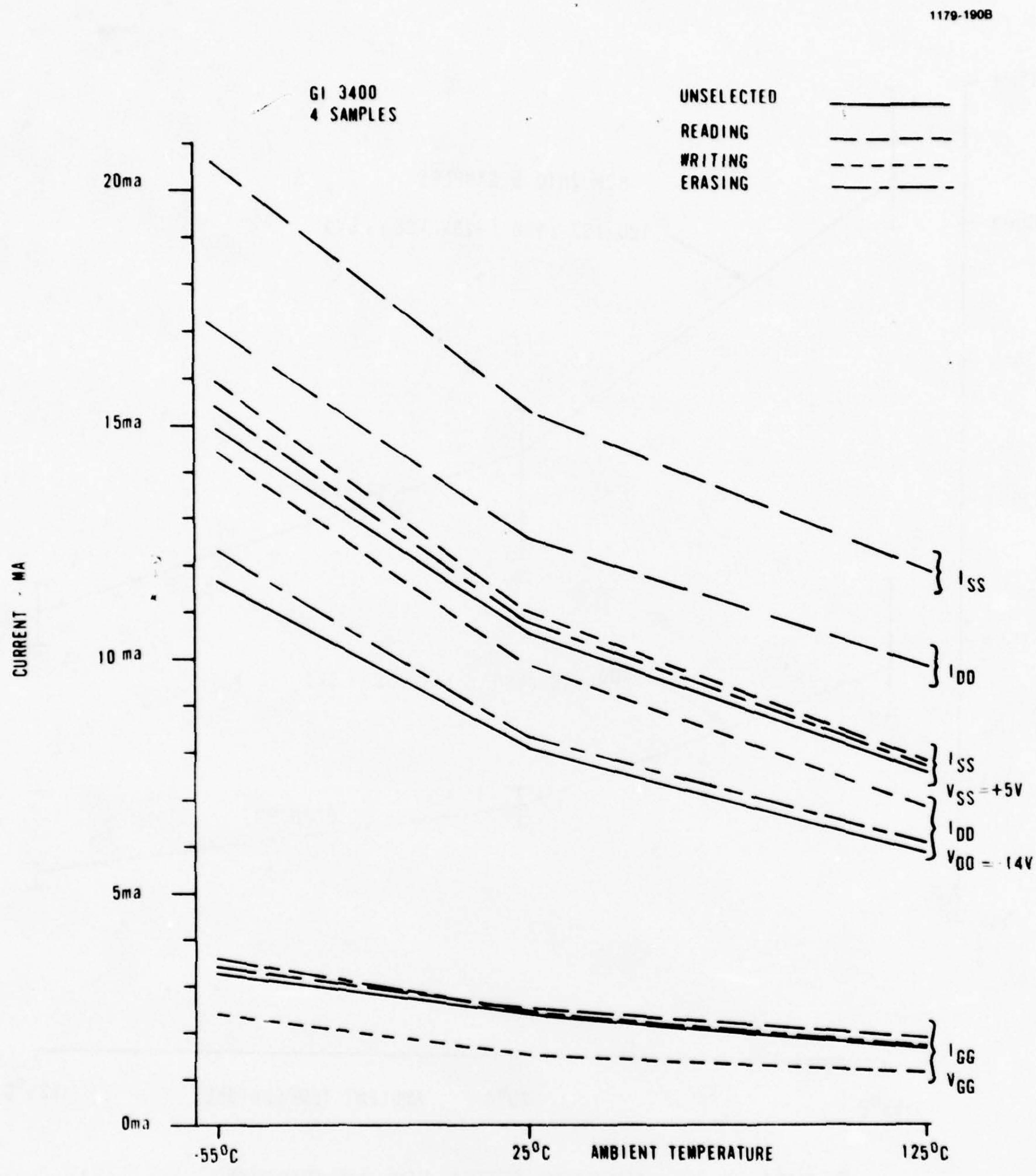


FIGURE 7-19. AVERAGE POWER SUPPLY CURRENT VS TEMPERATURE (AMBIENT) FOR NCR 2451

POWER SUPPLY AVE CURRENT vs TEMPERATURE

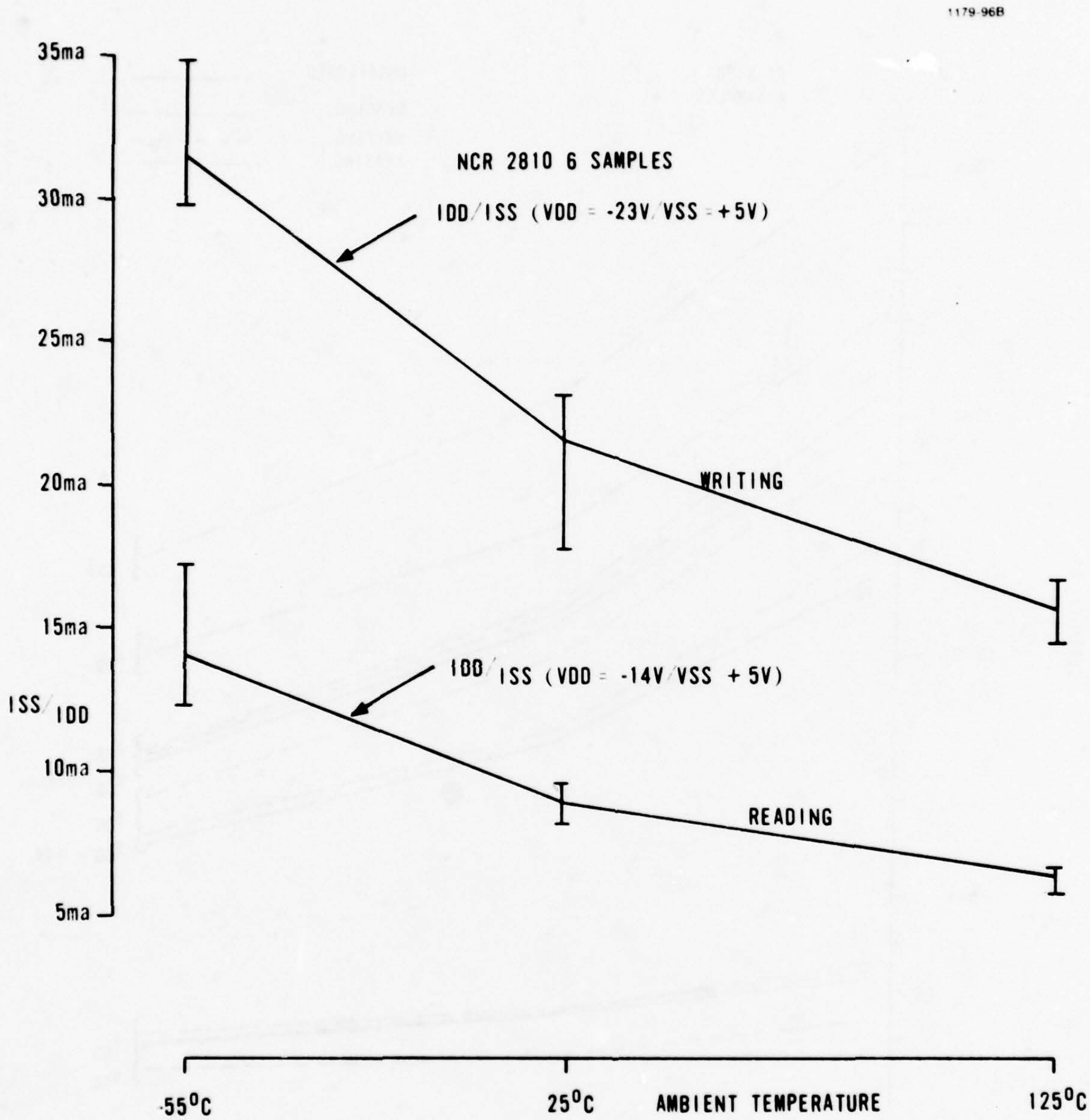


FIGURE 7-20. AVERAGE POWER SUPPLY CURRENT VS TEMPERATURE (AMBIENT) FOR NCR 2810

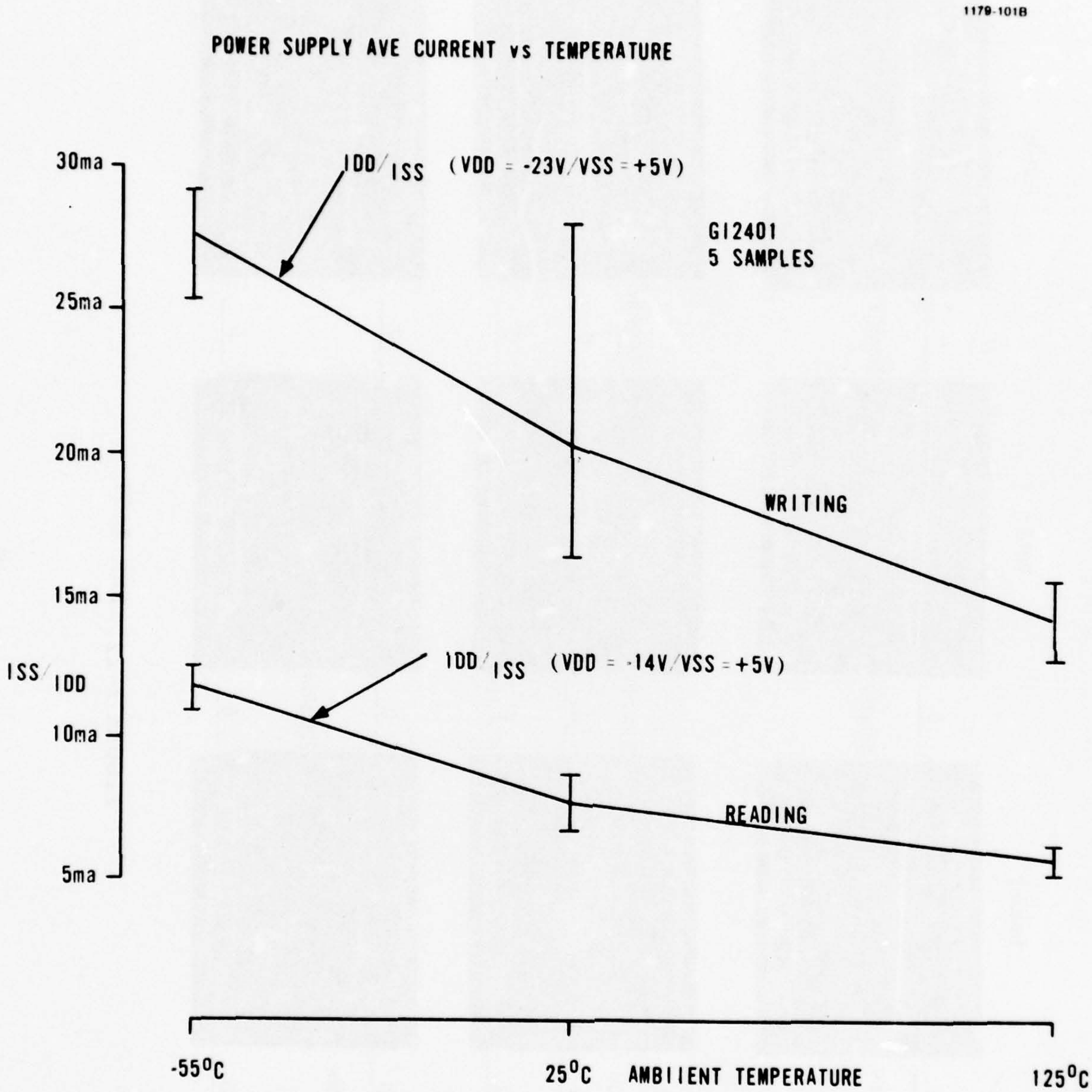


FIGURE 7-21. AVERAGE POWER SUPPLY CURRENT VS TEMPERATURE AMBIENT FOR GI2401

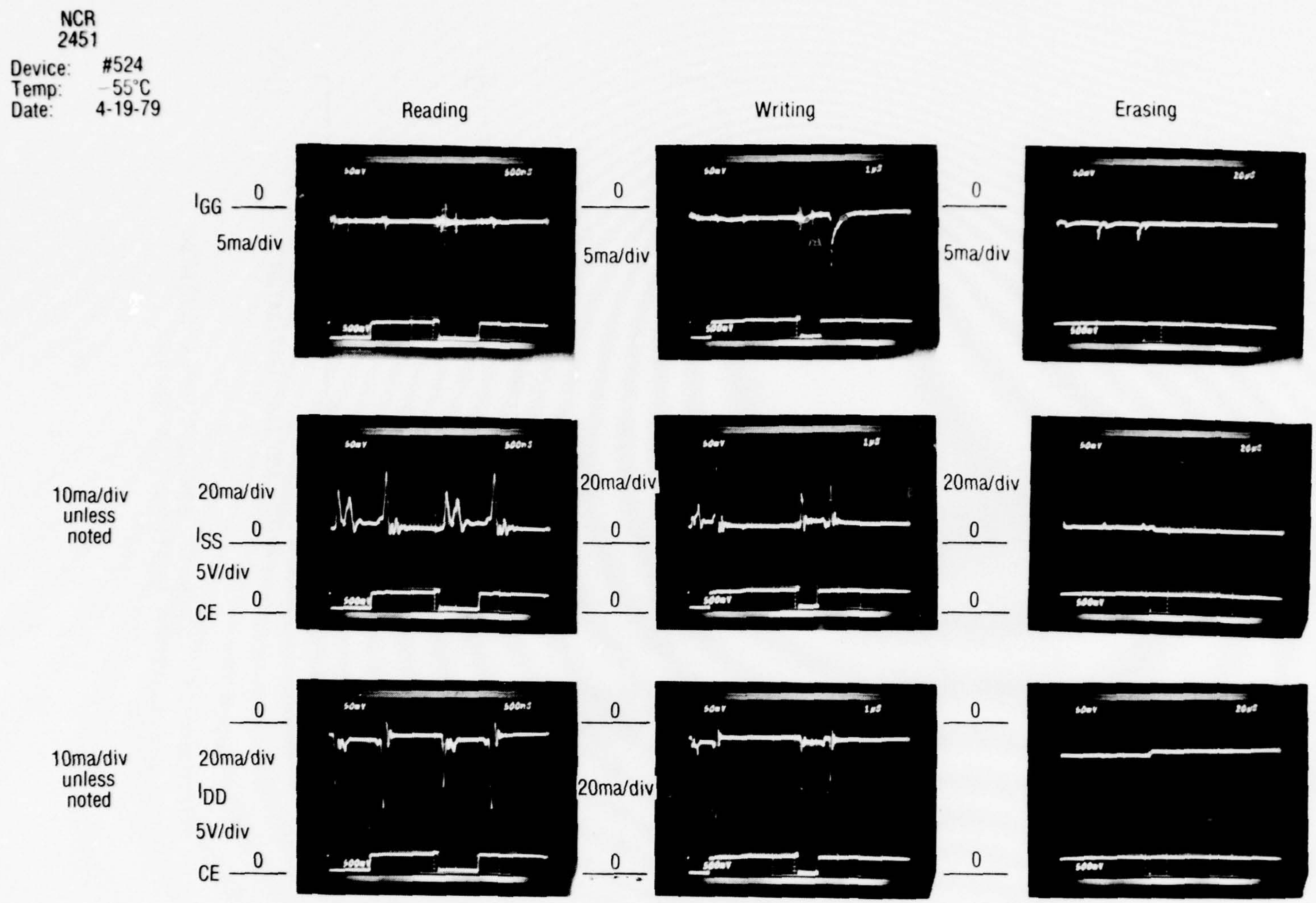


FIGURE 7-22. NCR 2451

2451
Device: #524
Temp: 25°C
Date: 4-18-79

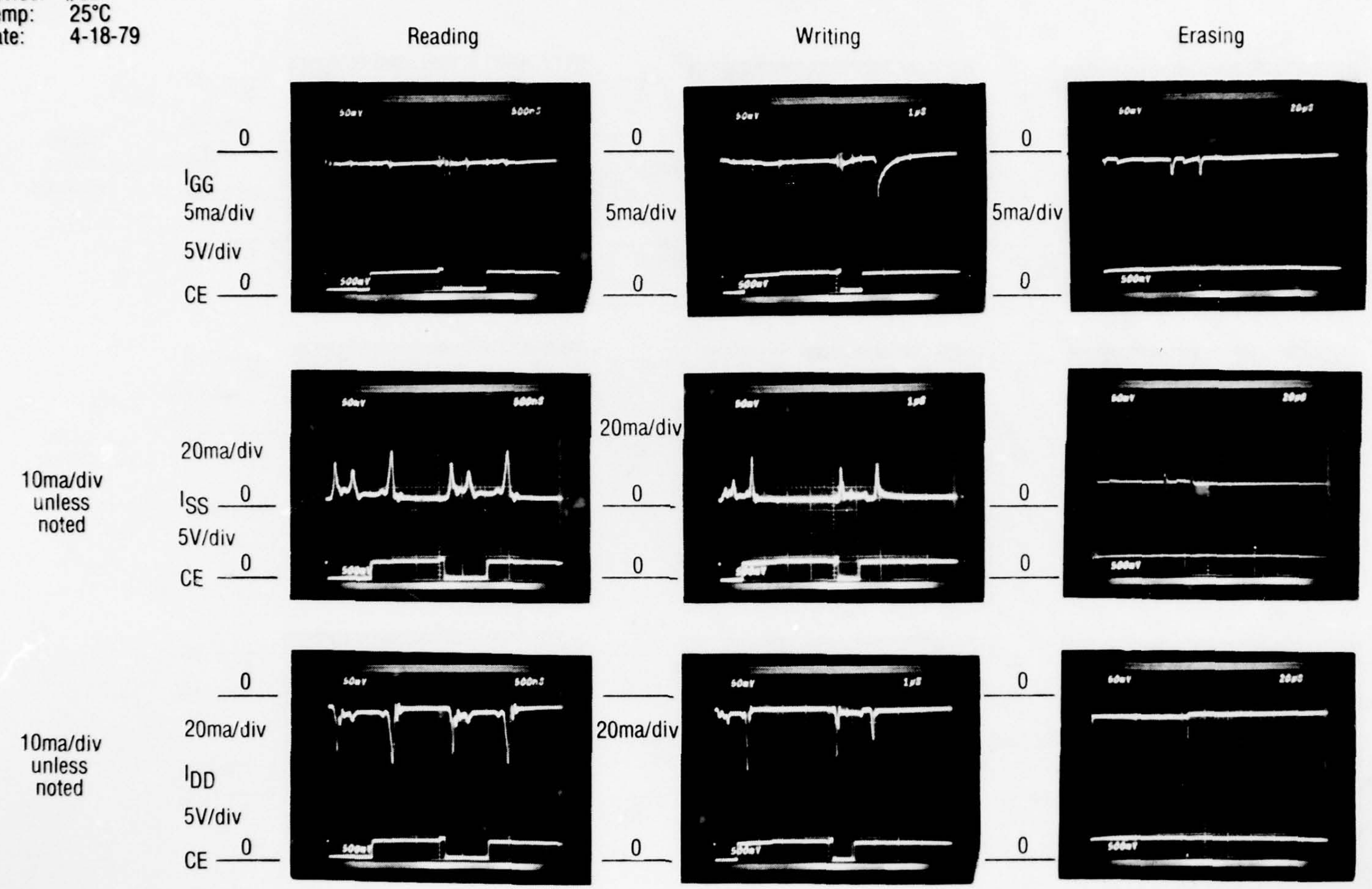


FIGURE 7-22. NCR 2451 (Cont)

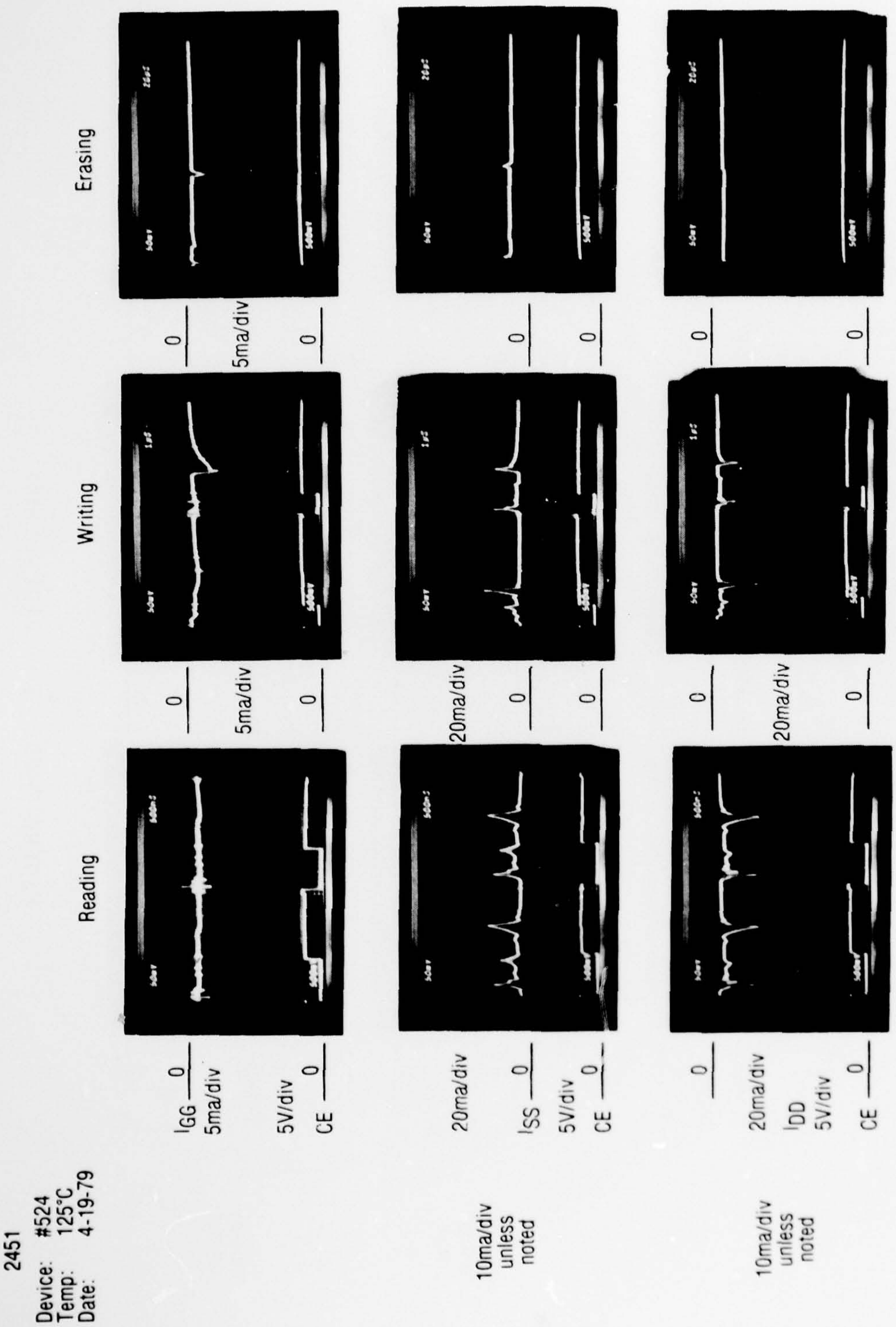


FIGURE 7-22. NCR 2451 (Cont)

3400
Device: #221
Temp: −55°C
Date: 5-4-79

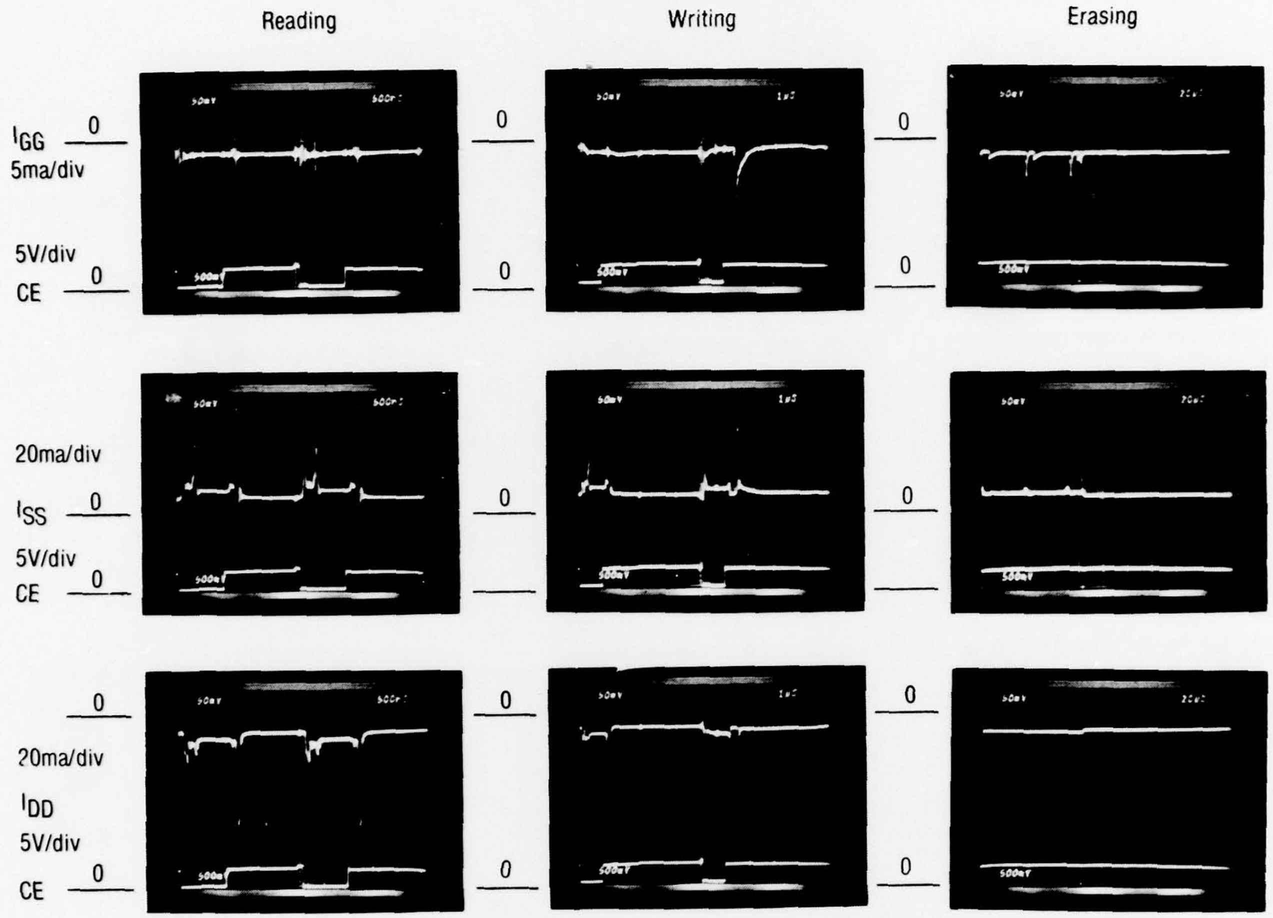


FIGURE 7-23. GI 3400

3400
Device: #221
Temp: 25°C
Date: 4-30-79

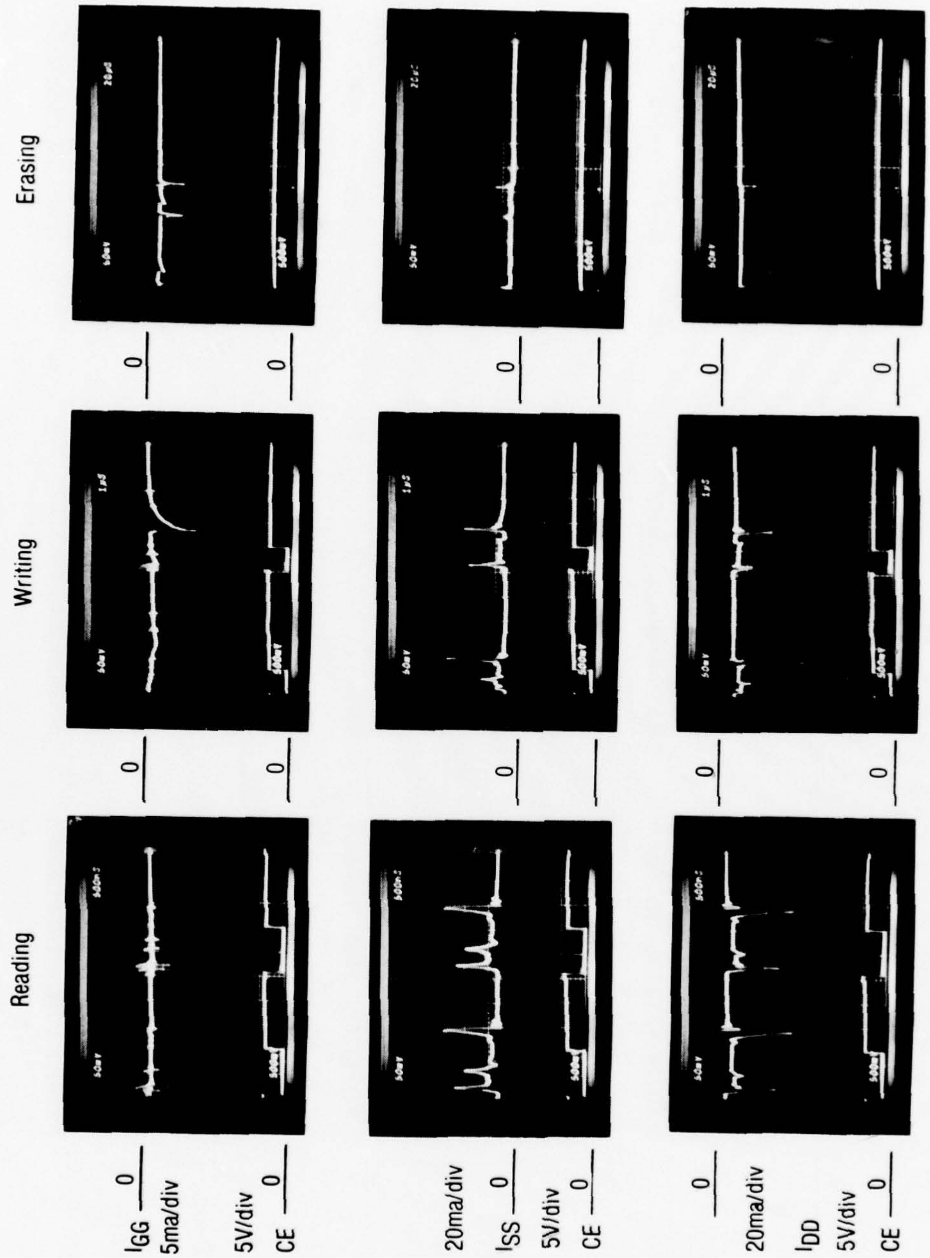


FIGURE 7-23. GI 3400 (Cont)

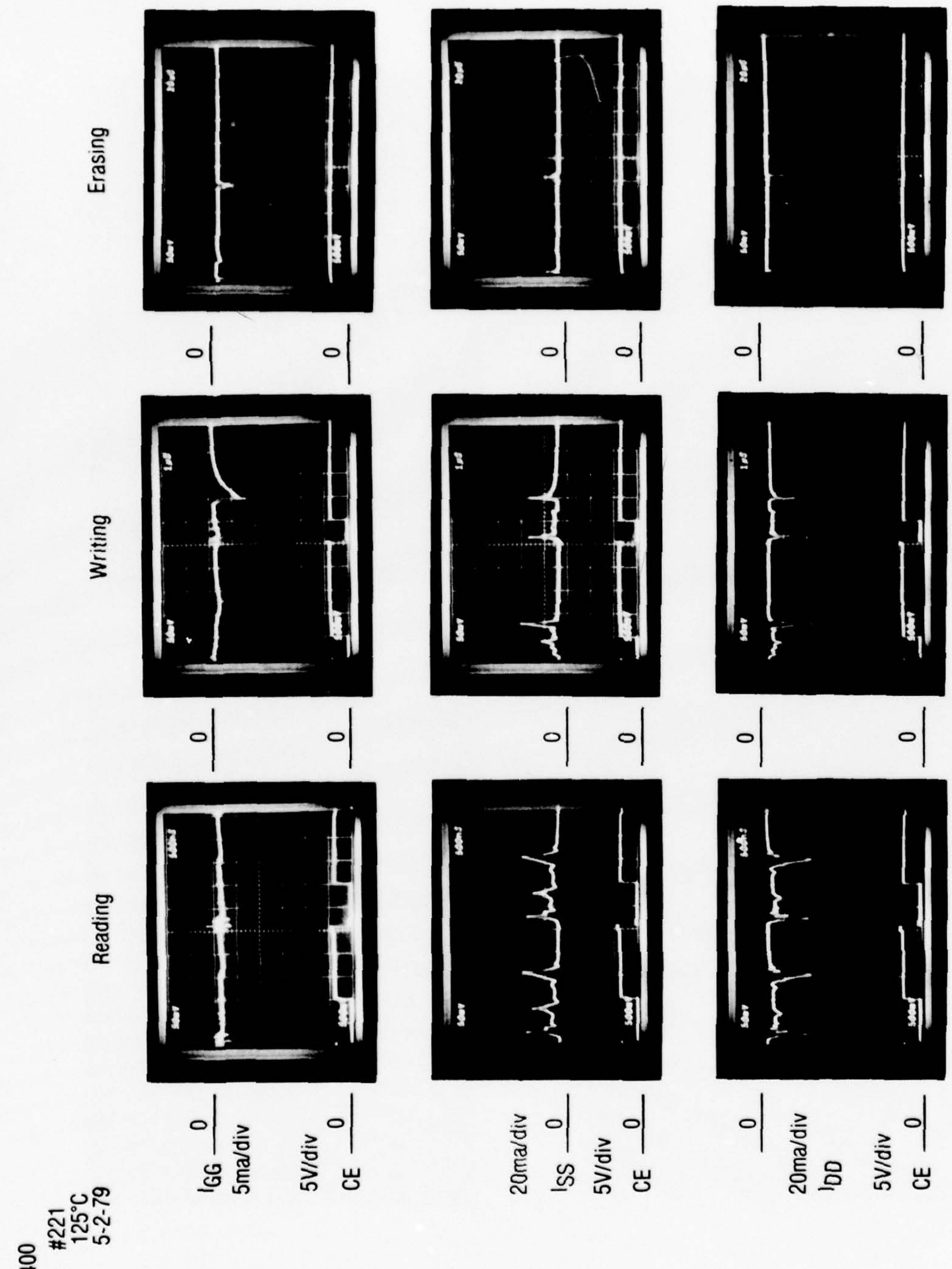


FIGURE 7-23. GI 3400

2810: #331
Temp: −55°C
Date: 4/10/79

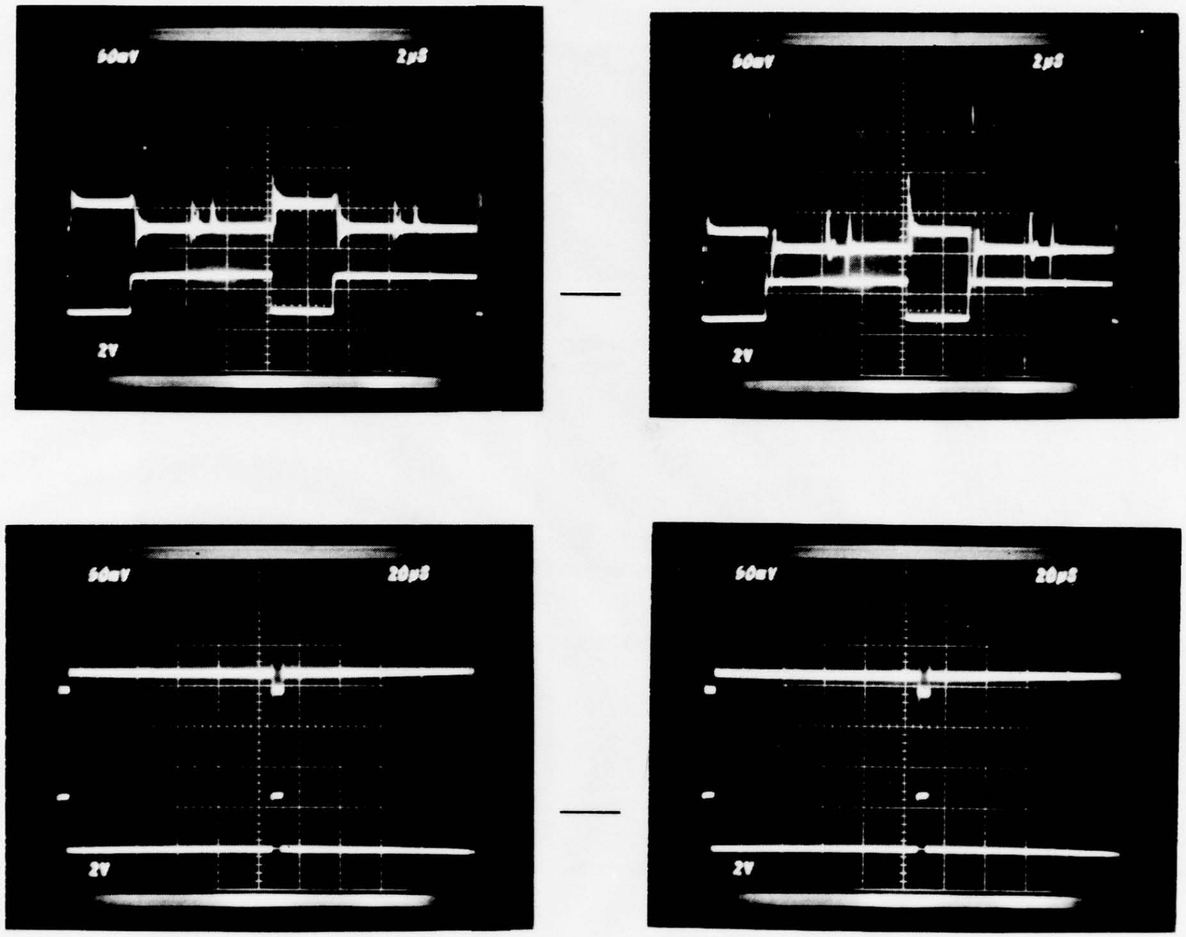


FIGURE 7-24. CURRENT WAVESHAPES, NCR 2810 (a) -55°C

2810: #331
Temp: 25°C
Date: 4-10-79

I_{DD} | I_{SS}

Read

10ma/div

0ma

0V

20V/div ϕ | 20V/div $\phi1$

Write

10ma/div

0ma

0V

20V/div $\phi1$

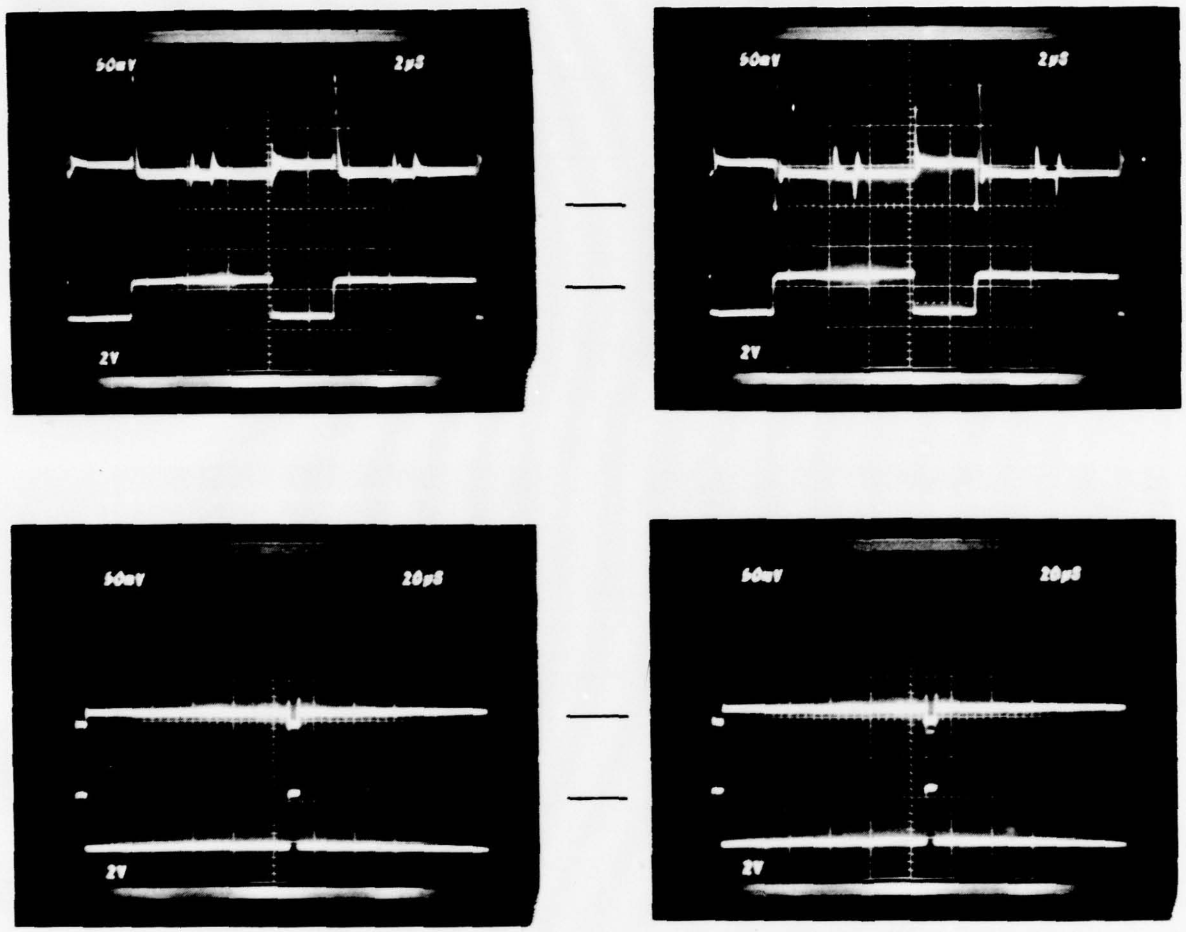


FIGURE 7-24. CURRENT WAVESHAPES, NCR 2810 (b) +25°C (Cont)

2810: #331
Temp: 125°C
Date: 4-11-79

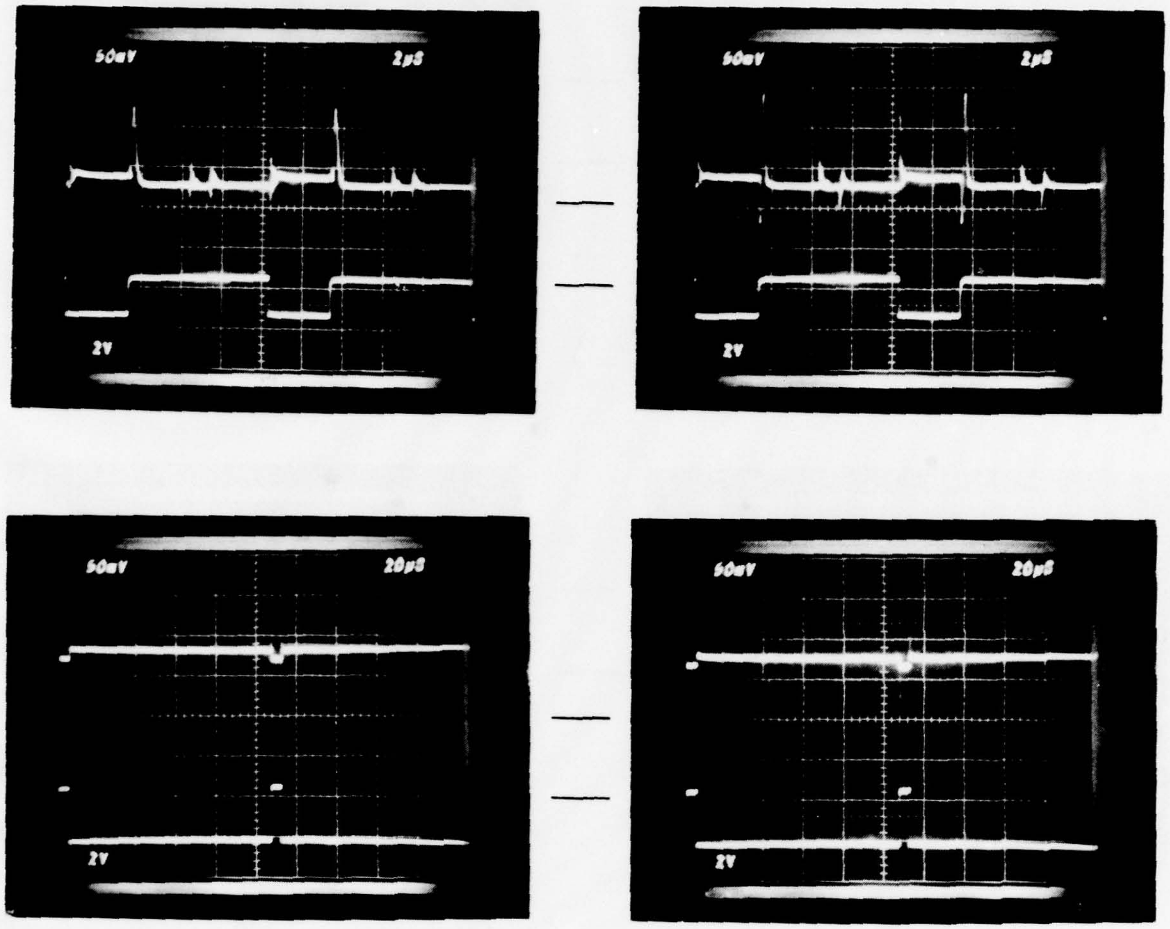


FIGURE 7-24. CURRENT WAVESHAPES, NCR 2810 (c) +125°C (Cont)

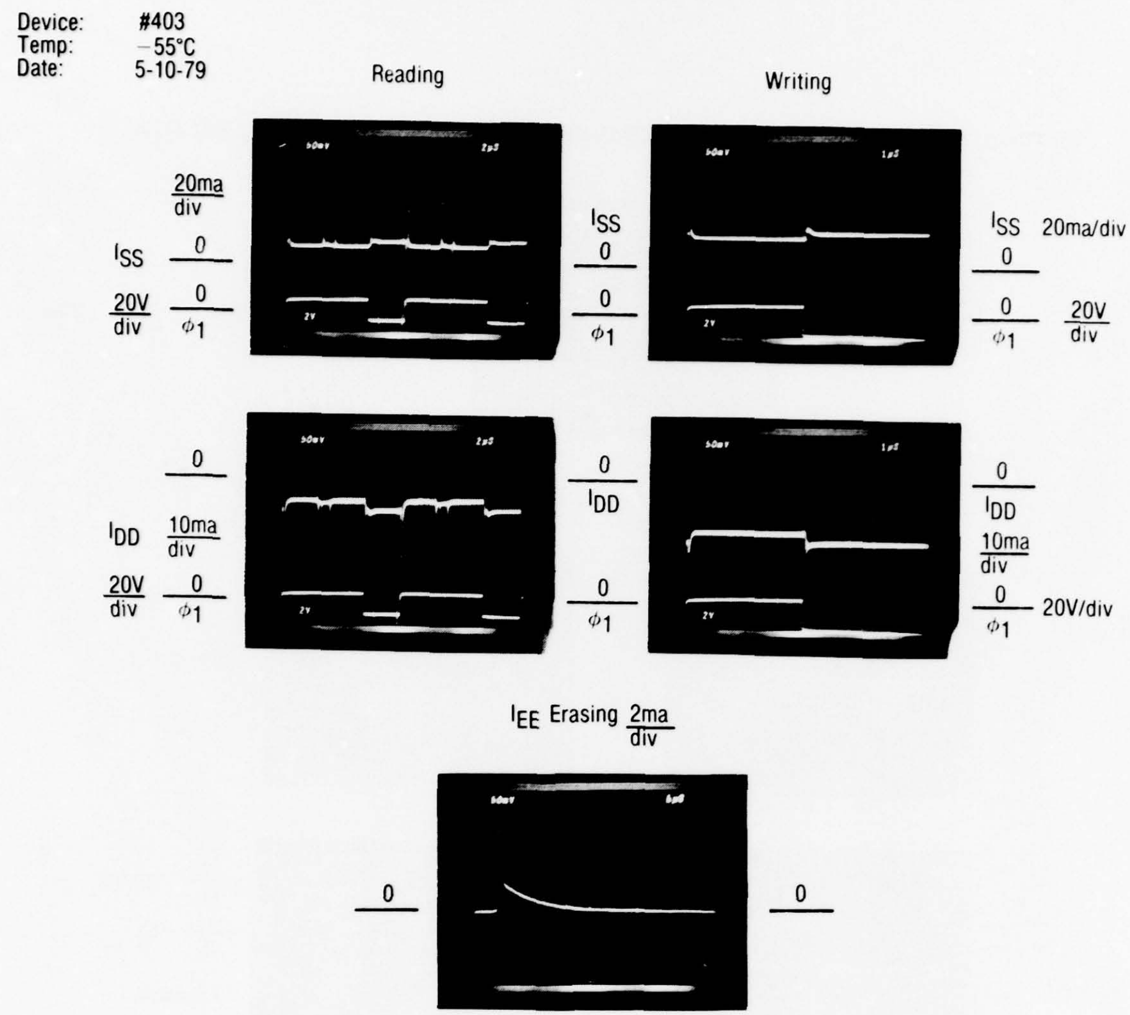


FIGURE 7-25. CURRENT WAVESHAPES, GI 2401 (a) -55° C

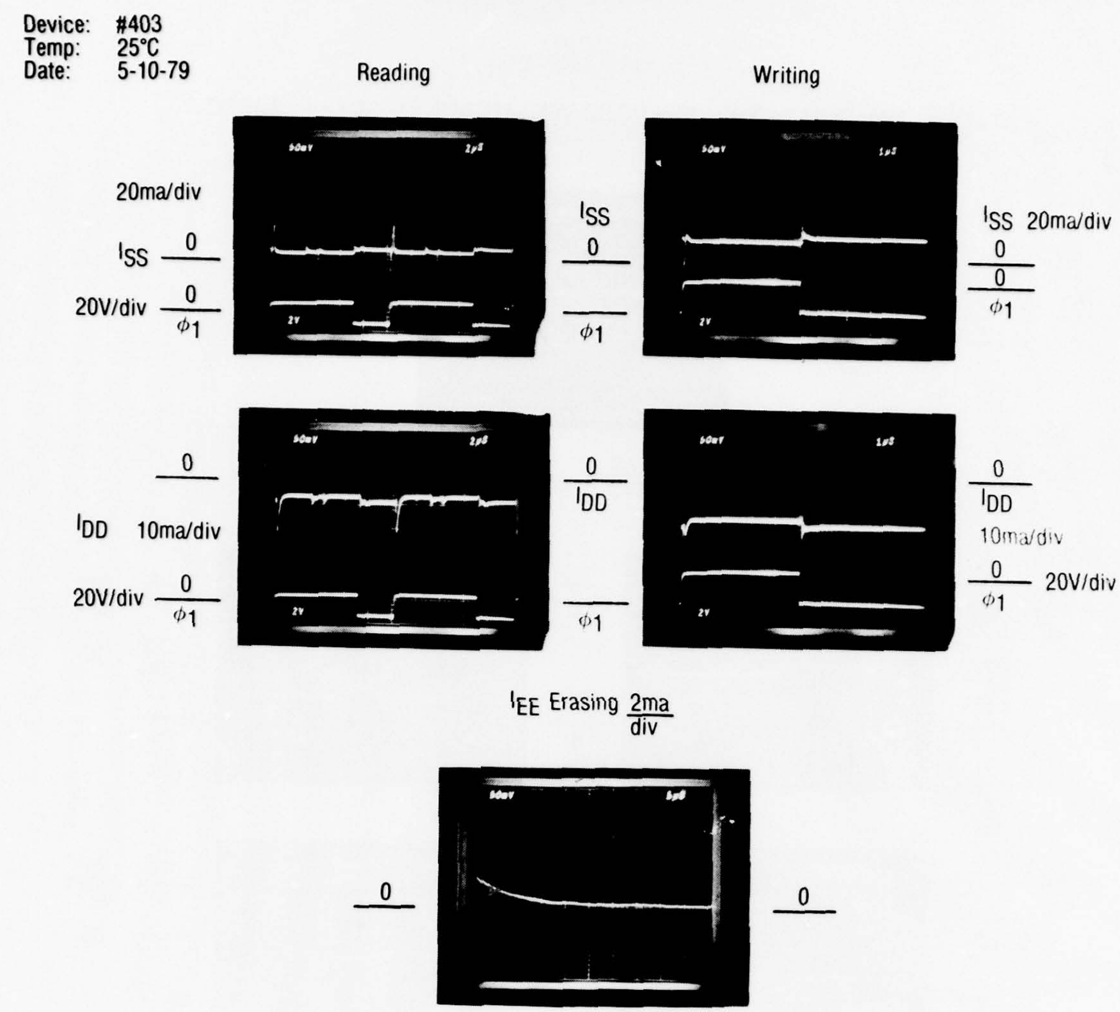


FIGURE 7-25. CURRENT WAVESHAPES, GI 2401 (b) 25°C (Cont)

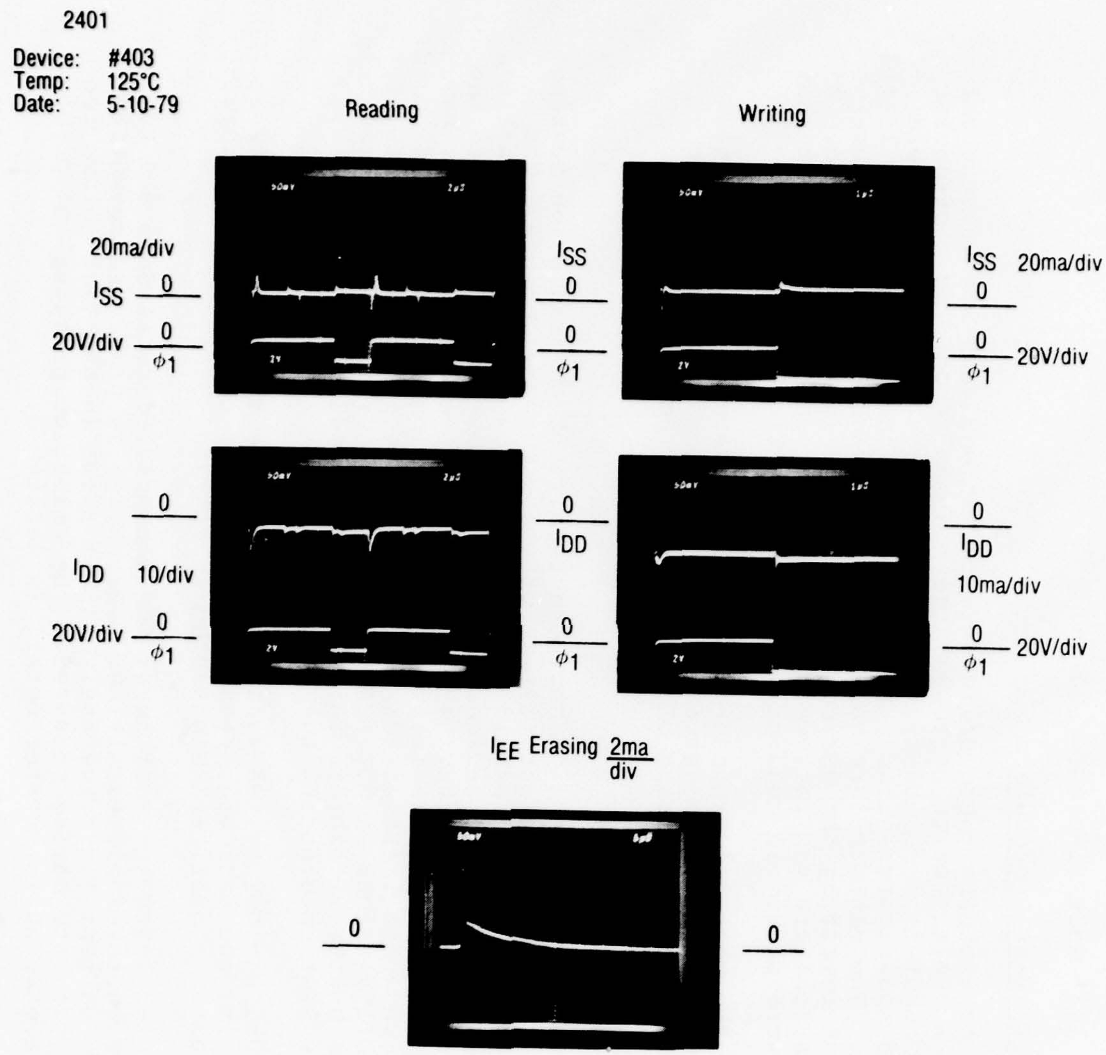


FIGURE 7-25. CURRENT WAVESHAPES, GI 2401 (c) 125°C (Cont)

7.1.4.1 Type of Test

Samples of each of the candidate devices were exposed successively to three increasing levels of dose rate. These rates were:

a. 10^6 Rads Si/sec for 20 ns.

b. 10^8 Rads Si/sec for 20 ns.

c. 10^{11} Rads Si/sec for 20 ns.

7.1.4.2 Test Procedure

Prior to exposing these devices to radiation, each was written into using a nominal write cycle and the minimum thresholds plotted for 10^5 seconds to simulate system use. Samples of each device were placed under normal bias conditions and exposed to the levels listed above. The minimum thresholds were then measured after exposure without rewriting the device and the change in threshold noted. A similar pattern was followed for samples of each device except that they were placed in conductive foam and left unbiased.

After the post-rad explosure thresholds were measured a retention plot was performed to determine any permanent influence on the retention characteristic of each device of the tests.

7.1.4.3 Results

Figures 7-26 through 7-33 show the results of the radiation testing on the retention characteristics of the candidate devices. The change in minimum threshold measurements show that small to neglible changes occur in all devices at the 10^{11} Rads Si/sec level with the low radiation levels having no measurable effect. The devices having one transistor plus reference row construction (i.e., NCR 2810 and GI 2401) show the least effect due to radiation. The single transister per cell versions (i.e., NCR 2451 and GI 3400) show greater threshold change but still exhibit relatively small radiation effects. No device lost data during the testing.

The 7053 was not tested during this test due to nonavailability at test time and lack of threshold measurements capability robs this testing of a qualitative measurement vehicle.

Table 7-2 lists the test level the accumulated total dose and the change in threshold resulting. The change in predicted retention (based on best fit curve analysis) is shown in the last column for the worst case device measured. The retention plotting and prediction are shown in greater detail in Section 8.

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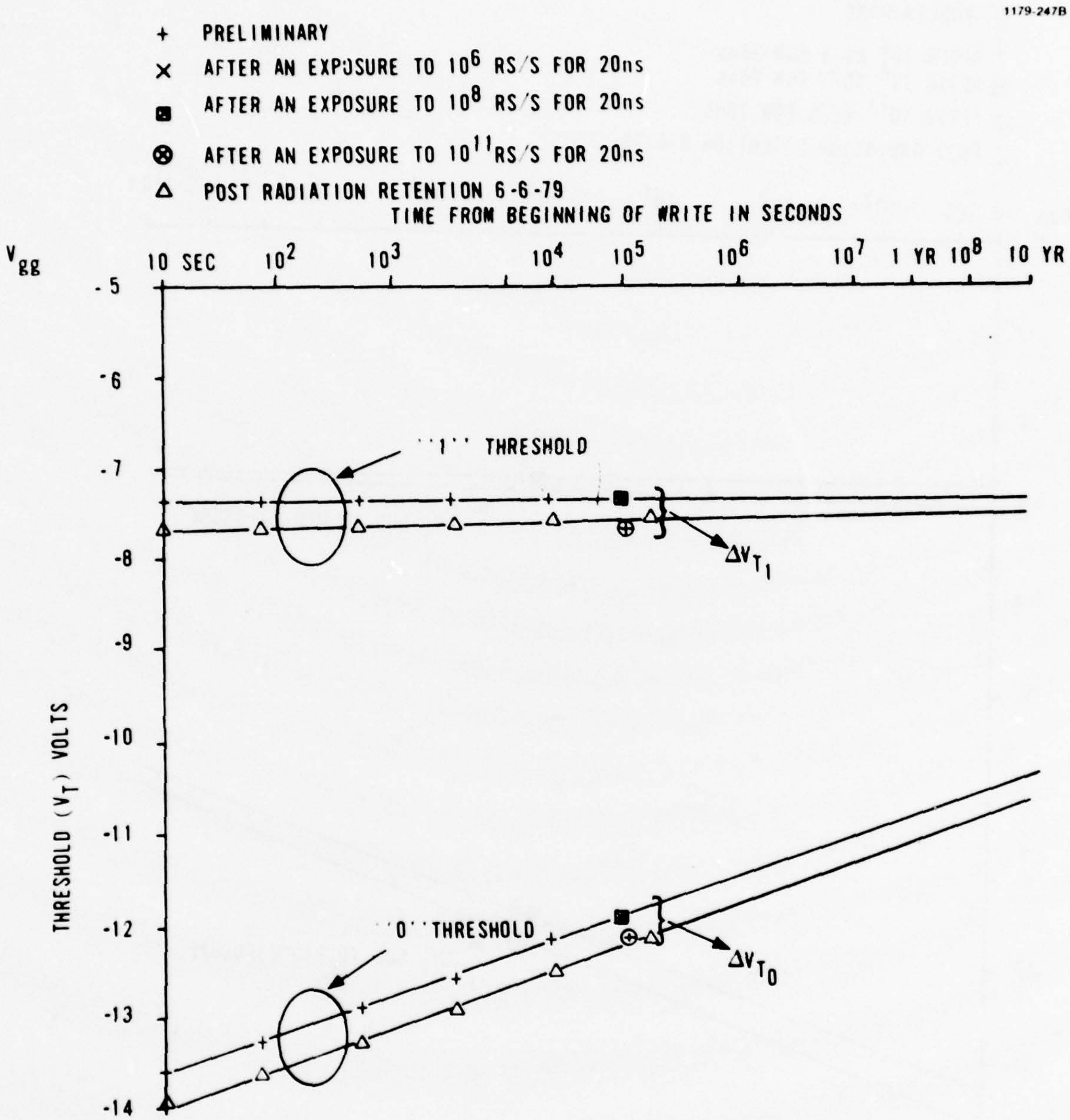

FIGURE 7-26. RADIATION EXPOSURE TESTING OF NCR2451 (SHORT CIRUCIT UNBIASED STATE)

1079-16060

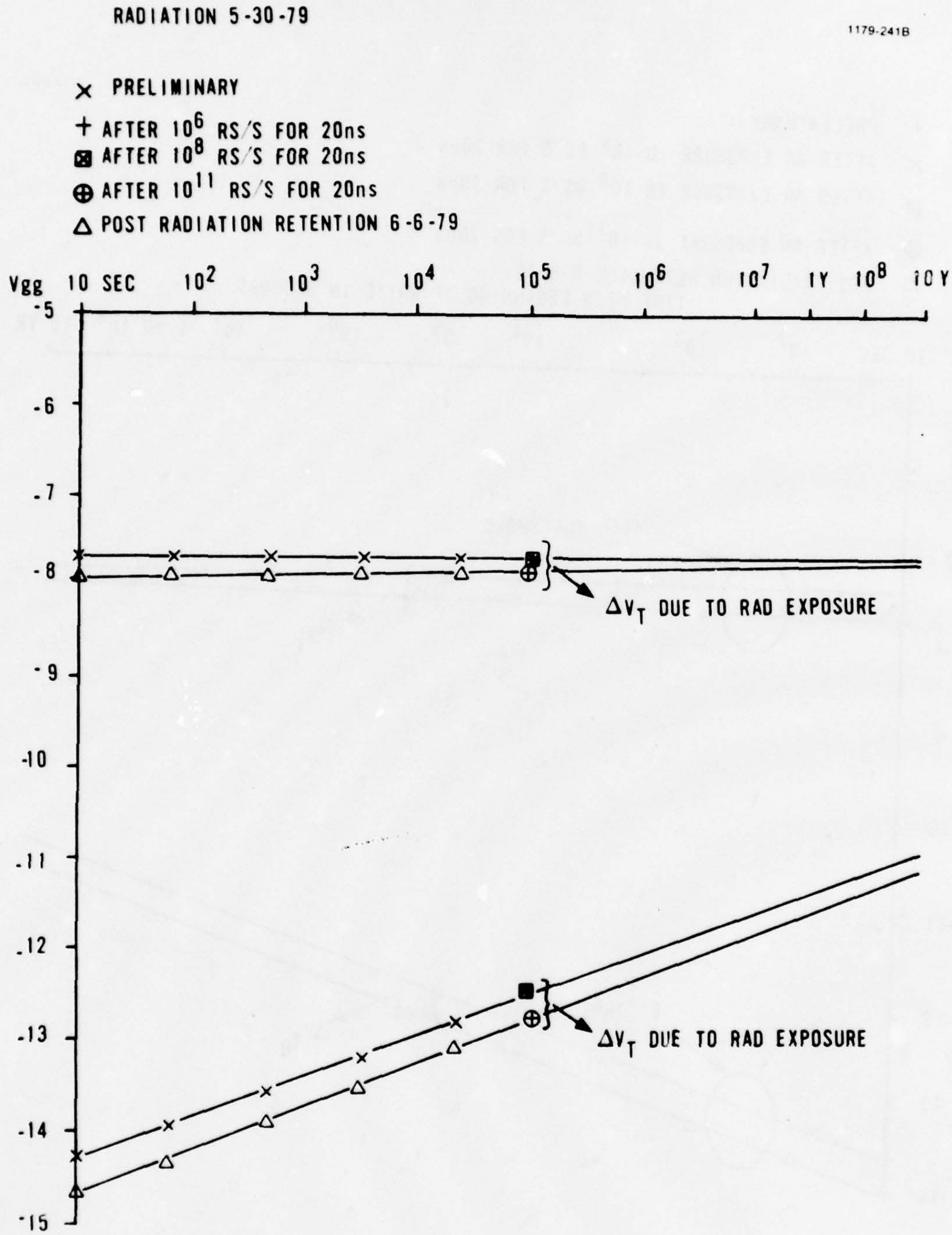

FIGURE 7-27. RADIATION EXPOSURE TESTING OF NCR2451 (BIASED STATE)

1079-16060

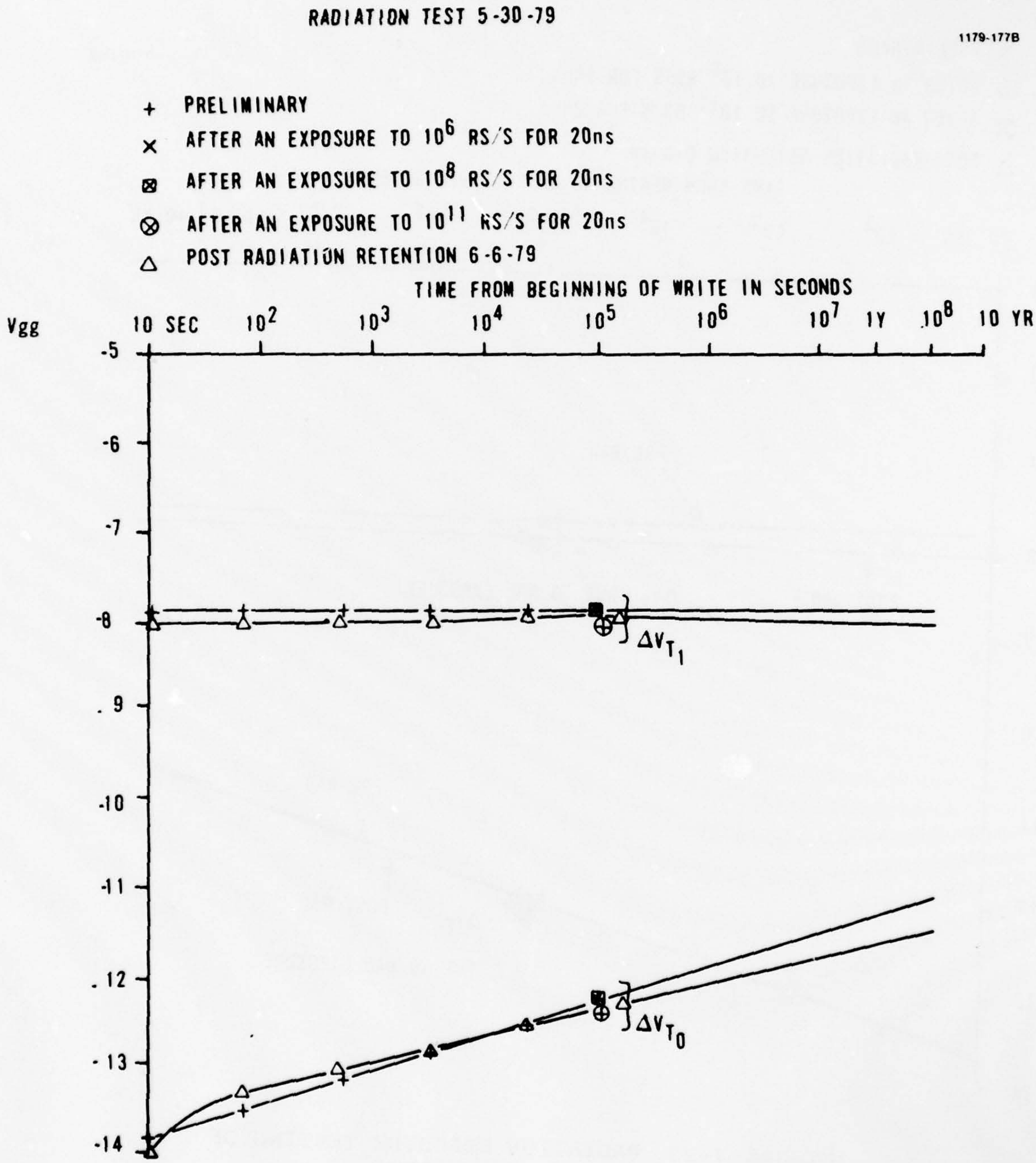

FIGURE 7-28. RADIATION EXPOSURE TESTING OF GI3400 (SHORT CIRCUIT UNBIASED STATE)

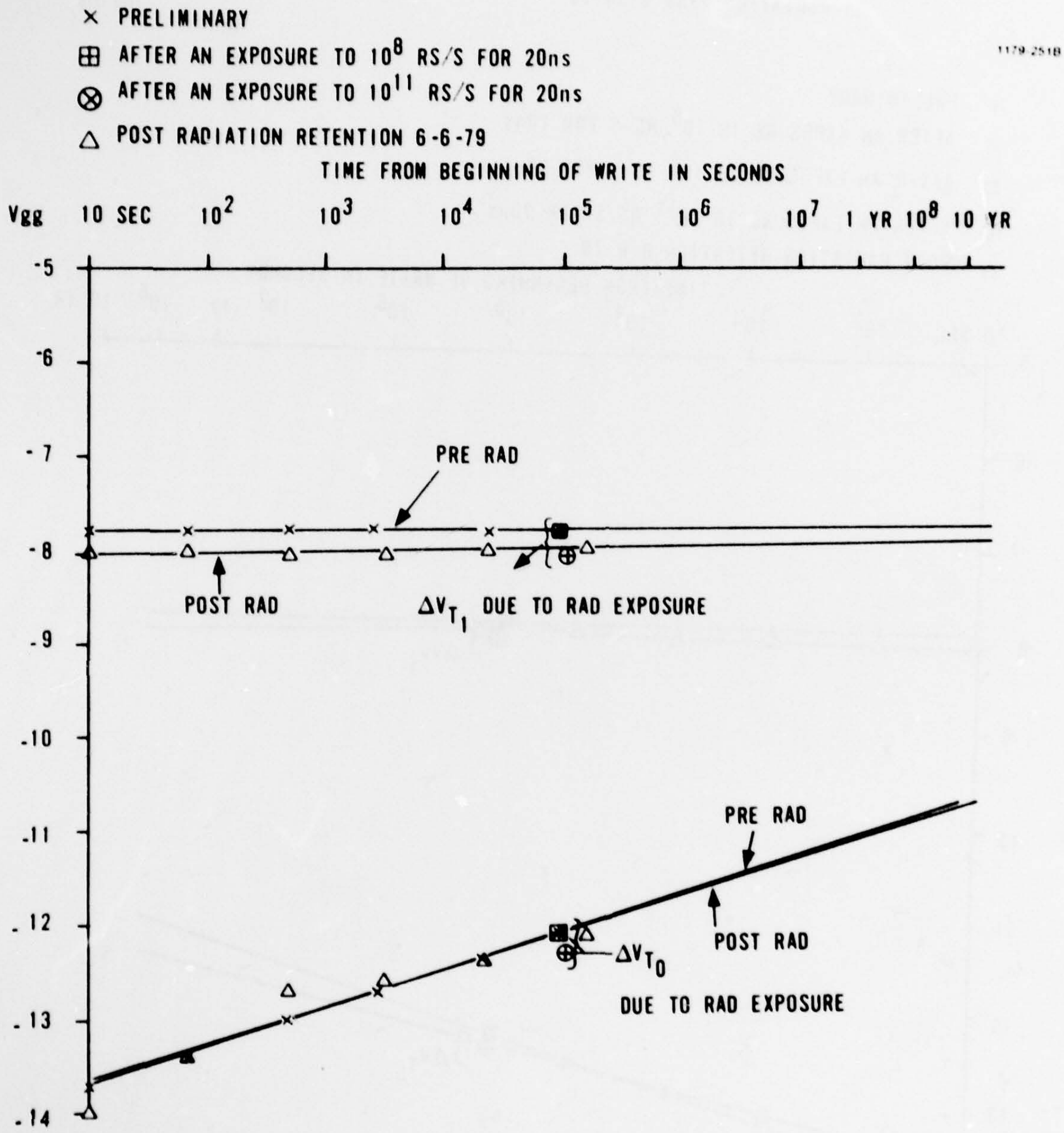

FIGURE 7-29. RADIATION EXPOSURE TESTING OF GI3400 (BIASED STATE)

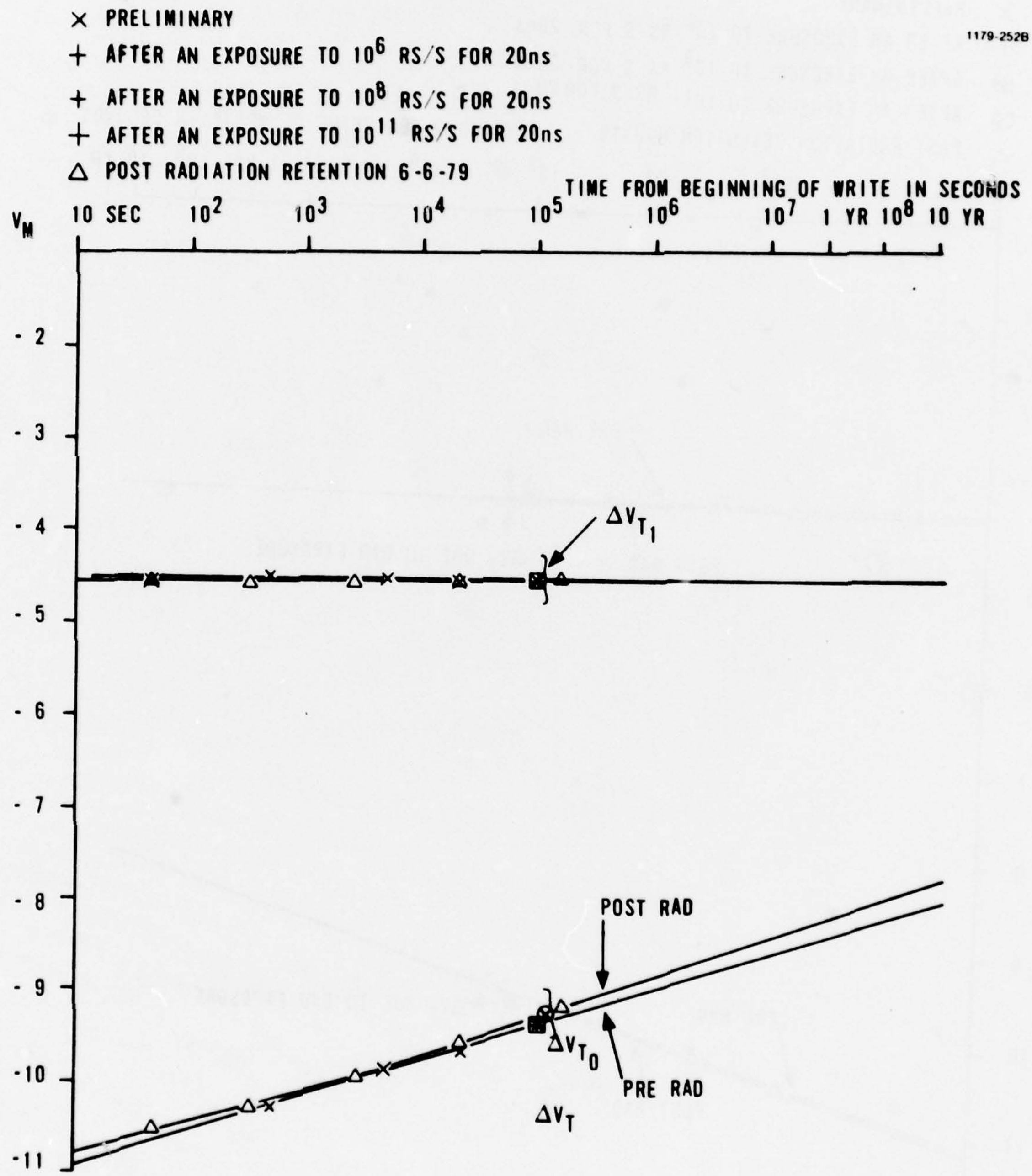

FIGURE 7-30. RADIATION EXPOSURE TESTING FOR NCR2810 (SHORT CIRCUIT UNBIASED STATE)

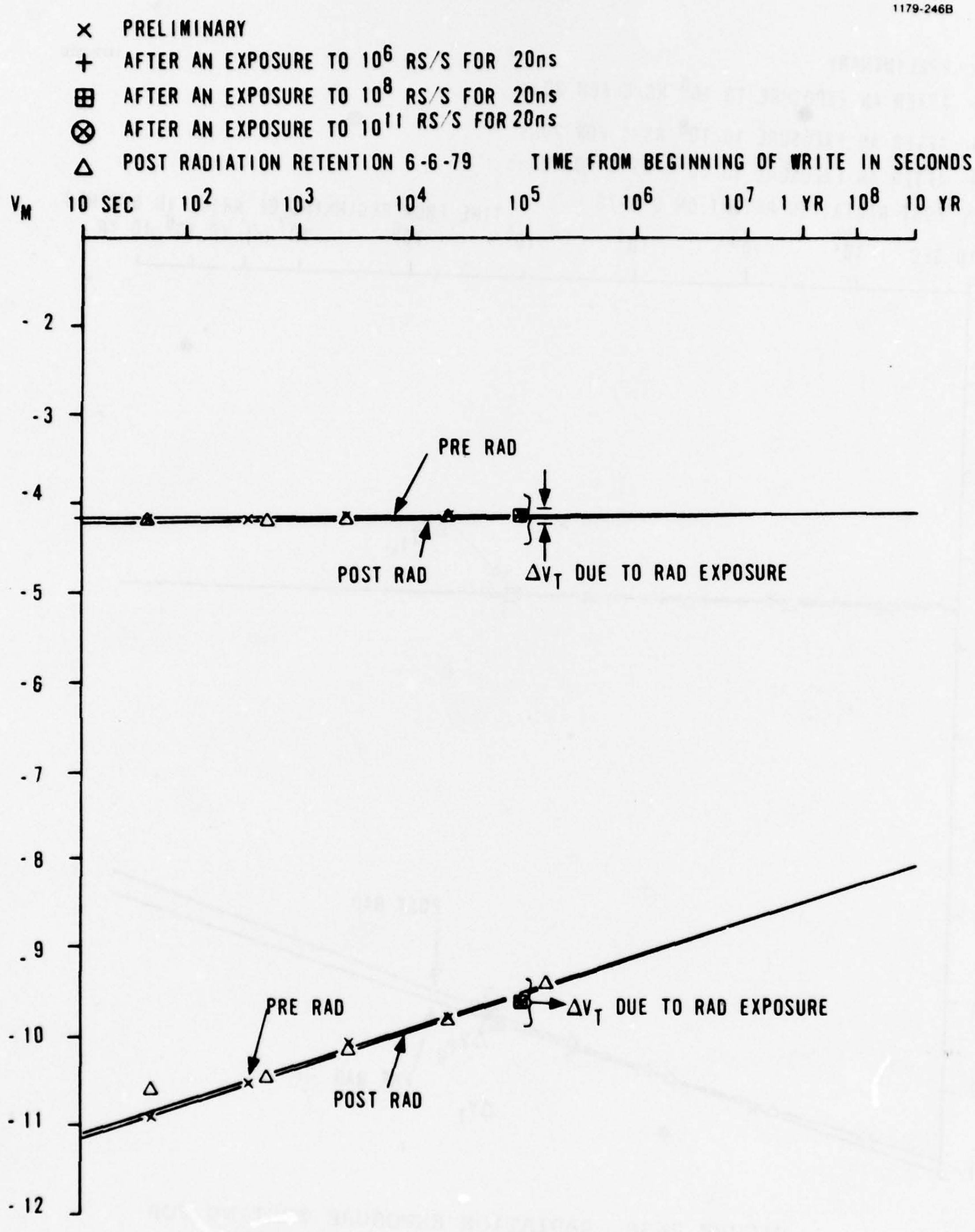

FIGURE 7-31. RADIATION EXPOSURE TESTING FOR NCR2810 (BIASED STATE)

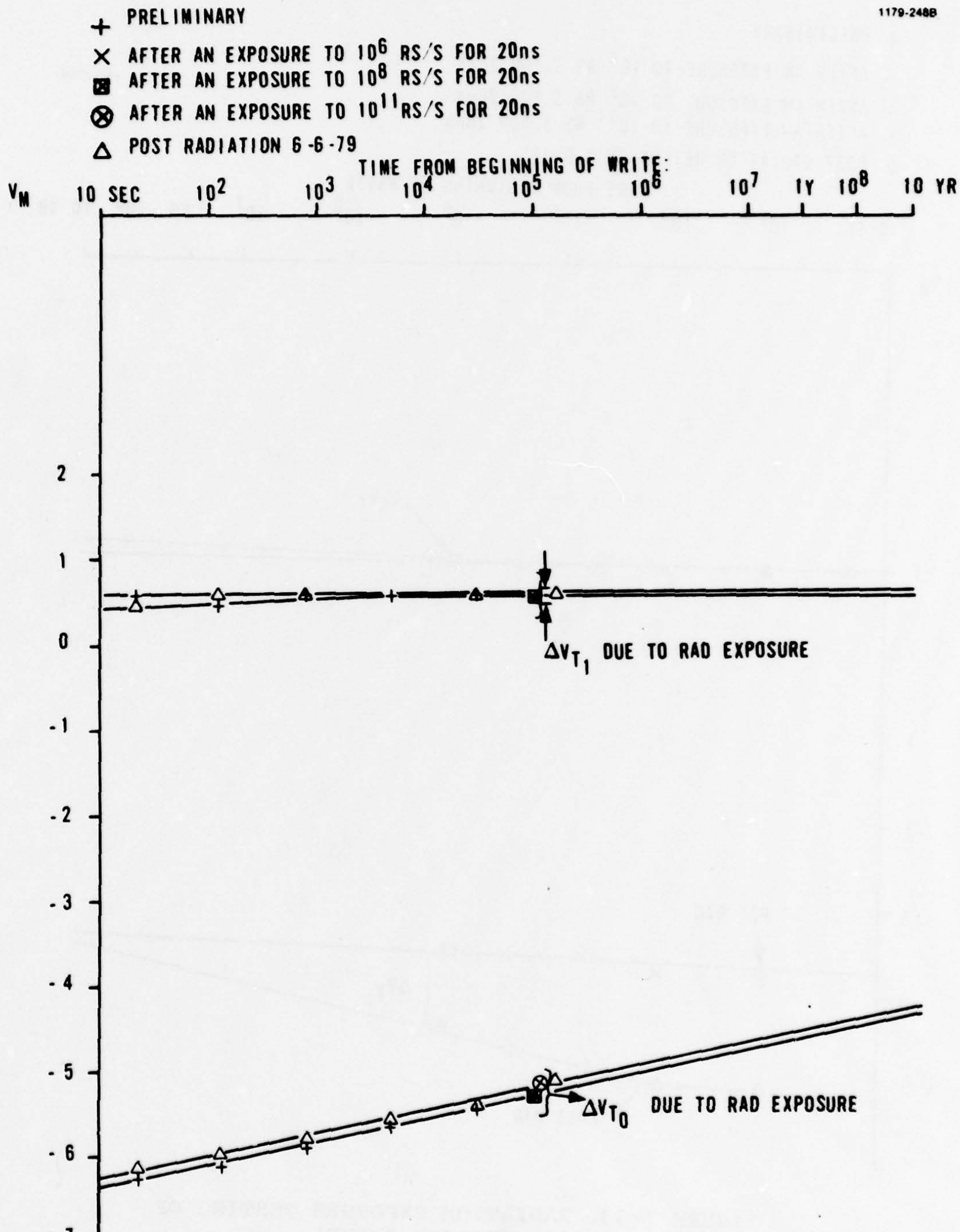

FIGURE 7-32. RADIATION EXPOSURE TESTING OF GI2401 (SHORT CIRCUIT UNBIASED STATE)

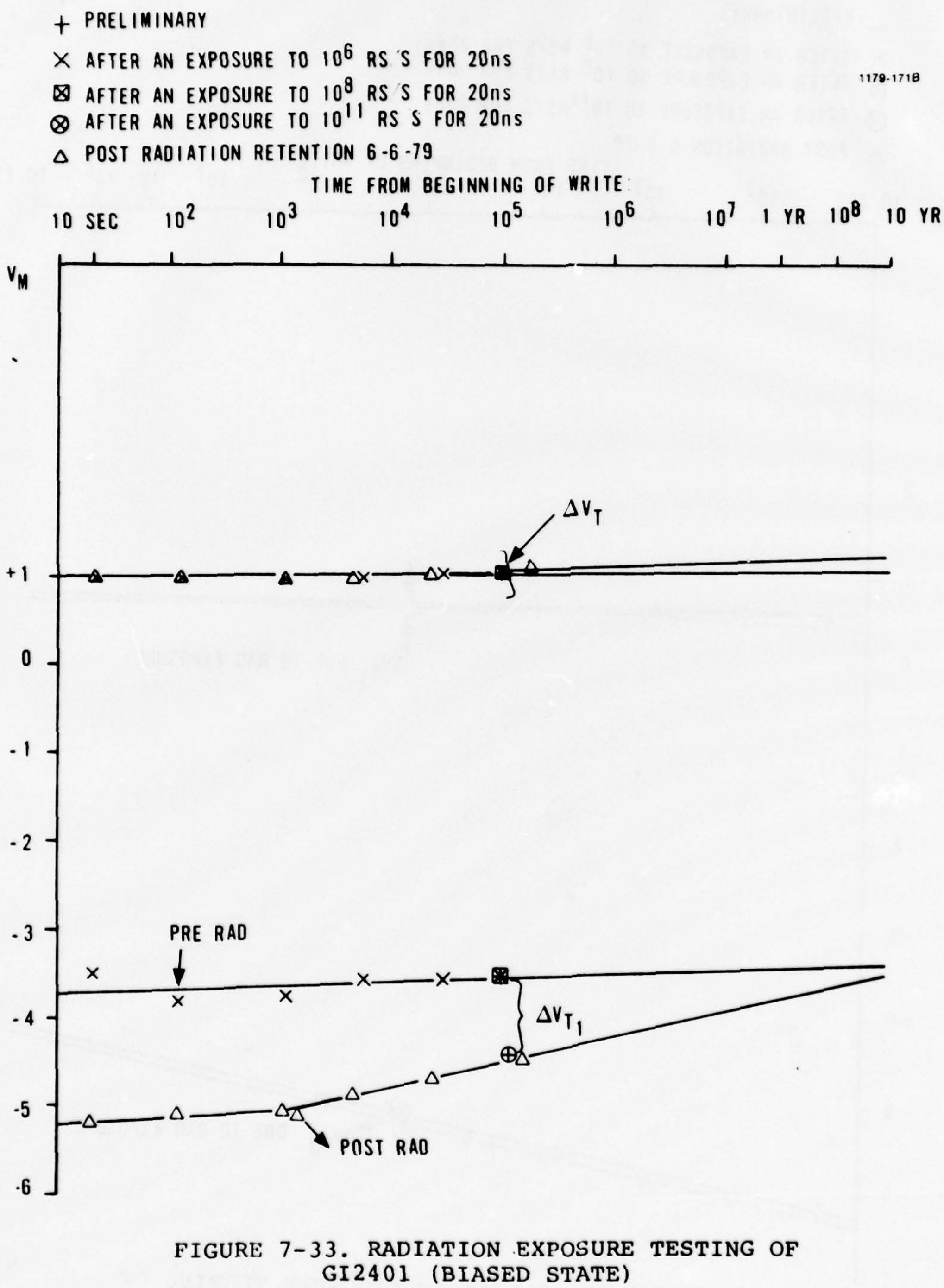

FIGURE 7-33. RADIATION EXPOSURE TESTING OF GI2401 (BIASED STATE)

7.1.4.4 Conclusions

The NCR2810 shows significantly better (i.e., less V_T) than the remaining devices followed by the 2401, 3400 and the 2451, in that order. All devices held their data during exposure and the slope of the retention curve was not effected by rad exposure. It should be noted that all devices had a total dose accumulation of 2000 rads. Total dose is anticipated to be the major criteria in radiation resistance to influence MNOS memories.

7.1.5 Writing Characteristics

The writing and erasing characteristics of MNOS memories are relatively slow and not usually considered a performance characteristic as much as a parameter in the retention and endurance characteristics. As a result in this phase of the MACI contract, relative writing characteristics were only considered in their relationship to the retention and endurance parameters.

TABLE 7-2. RESULTS OF RADIATION TESTING OF MNOS DEVICES FOR MACI - EAROM PROGRAM

Device	Rad Exp.	Total Dose	Initial V_T		Change V_T		Retention		Average Change V_T/Decade-Zeros	
			Ones	Zeros	Ones	Zeros	Pre	Post	Pre	Post
2401 #406	10^6	0.02	0.58	-5.14	0	0				
	10^8	2.02	0.58	-5.14	-0.2	0	1.49 $\times 10^{20}$	1.72 $\times 10^{20}$	0.2774	0.2763
	10^{11}	2002.02	0.56	-5.14	0	0.033				
2501 #507	10^6	0.02	-7.7	-12.48	0	0.02				
	10^8	2.02	-7.7	-12.45	0.02	0.01	1.15 $\times 10^{11}$	2.36 $\times 10^{11}$	0.4584	0.4773
	10^{11}	2002.02	-7.88	-12.72	-0.22	-0.28				
3400 #217	10^8	2.0	-7.8	-12.1	0	0.02	4.75 $\times 10^9$	5.01 $\times 10^9$	0.4237	0.3700
	10^{11}	2002.0	-7.8	-12.08	-0.22	-0.18				
2810 #334	10^6	0.2	-4.14	-9.5	0	0				
	10^8	2.02	-4.14	-9.5	0	0.02	4.19 $\times 10^{14}$	8.28 $\times 10^{14}$	0.4143	0.4207
	10^{11}	2002.02	-4.14	-9.48	-0.02	0.08				

Section 8

MNOS UNIQUE CHARACTERISTICS

The parameters studied in this section are those peculiar to MNOS Technology or other similar nonvolatile semiconductor technologies. These parameters are:

a. Static Retention. Defined as the minimum length of time after writing that a "1" or "0" stored in memory can no longer be determined by the sense amplifier or has switched state. This definition requires the device not be read continuously but remain idle between periodic checks to determine state. It is essentially a time-delay measurement with the primary forcing function being time.

b. Read Disturb Detention. Defined as the minimum number of read access cycles on a particular memory cell after writing that a stored "1" or "0" can no longer be determined by the sense amplifier or has switched state. The forcing function in this case is the number of read cycles.

c. Endurance. MNOS (and other nonvolatile semiconductor memory technologies) exhibit degradation of some of their characteristics as a function of the number of erase/write cycles that are performed per individual memory cell. This phenomenon is called Endurance and is measured primarily in terms of the relationship between the retention characteristic and the number of erase/write cycles. The ability of a memory cell to retain data over extended periods of time is increasingly impaired as a direct function of the number of write/erase cycles performed on it.

   The endurance is, therefore, defined as the change in retention of a device after a fixed number of write/erase (W/E) cycles. A significant point is that evaluation of this parameter must be done at the memory cell level as other cells on the same chip which are written or erased differently will react in a different way. The number of W/E cycles used to gauge the Endurance capability of a device will vary from device to device depending on their construction and purpose.

   Other parameters could be used to measure endurance, such as access time and initial threshold window change, but these are also affected by many other effects making the correlation more tenuous. Care also has to be taken in performing endurance testing to insure that proper and well documented write/erase

cycle timing and bias are used relevant to the device. This is particularly so if comparative studies between similar devices is to be valid.

8.1 STATIC RETENTION

Using the definition above, a means of predicting when a particular device will reach an end of retention point becomes immediately significant to a comparative analysis. Since the MNOS memories rely on trapped charge as the means of retaining data and the time discharge function is logrithmic in nature, the memory retention is plotted on semi-log graph paper. This results in a best fit linear plot extrapolated to the end of life points of the device.

Figure 8-1a shows a typical plot of a 8K bit MNOS device. The vertical Vm while not being the threshold directly is a voltage measured at an output pin on the device which is directly proportional to threshold voltage. By assuming $V_m = V_t$, Figure 8-1 shows the decay of V_t as a function of time. The upper curves represents the most negative or maximum value of the "1" threshold of the memory device. The lower curves represent the minimum or least negative value "0" threshold of any cell in the device. By using these minimum values, the systems equivalent of the first "hard" error is simulated. The "1" state, for purposes of this report, is defined as that threshold state of a memory cell which will cause, when measured by the sense amplifier, the output to be in the V_{OH} or "high" state. In all the candidate devices, except the 7053, this refers to the high conductance, low threshold state. The "0" state is defined then to cause the output to be in the V_{OL} or "low" state, which in the above devices translates a high threshold, low conductance state.

In the 7053 the use of a differential memory cell while maintaining the relationship between the output state and the cell state, the implementation is different. In this case different sides of the differential cell are in the low conductance (high threshold) state depending on the data sense.

In all devices the erase procedure puts all devices in the high conductance (low threshold) state. The writing process causes selected memory cells to switch to the low conductance (high threshold) state. In the 7053 the side of the two transistor cell which switches is dependent on the input sense.

Figure 8-1 shows typical plots of MNOS device thresholds measured from the time the device was written. The change in V_T with time reflects the loss of stored charge as a result of tunneling through the oxide to the substrate. From this graph the retention behavior of the device can be predicted by extrapolating the curve out to the desired time.

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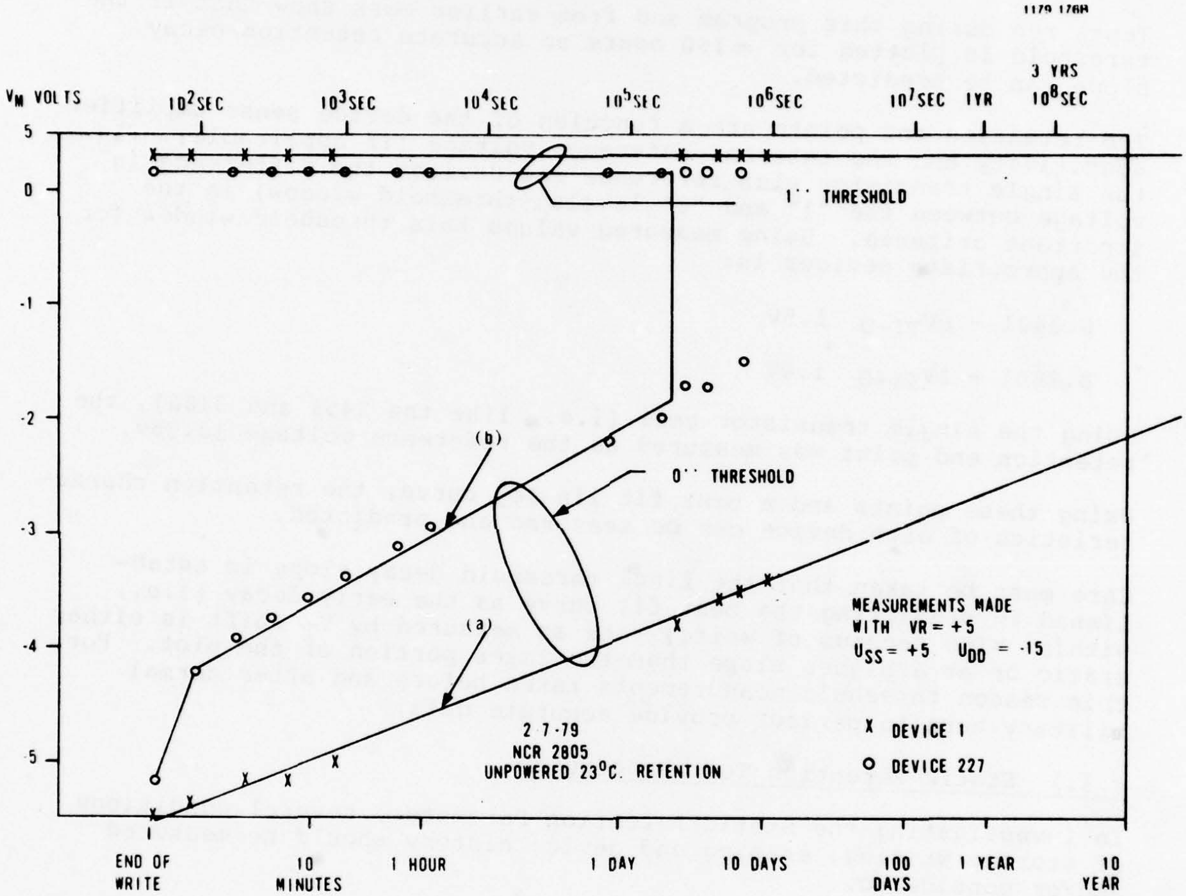

FIGURE 8-1. TYPICAL RETENTION PLOT

It is also apparent that devices that exhibit poor retention characteristics (i.e., like device No. 227) can be spotted by this testing and eliminated (i.e., screening criteria).

Tests run during this program and from earlier work show that if the threshold is plotted for ≈160 hours an accurate retention decay slope can be predicted.

The retention end points are a function of the device sense amplifier sensitivity and the internal reference voltage (if applicable). In the single transistor plus reference row devices the difference in voltage between the "1" and "0" levels (threshold window) is the important criteria. Using measured values this threshold window for the appropriate devices is:

0.2401 - ΔV_{TI-O} 1.5V

0.2801 - ΔV_{TI-O} 1.4V

Using the single transistor cell (i.e., like the 2451 and 3400), the retention end point was measured as the reference voltage ±0.35v.

Using these points and a best fit lin-log curve, the retention characteristics of each device can be measured and predicted.

Care must be taken that the final threshold decay slope is established in predicting the best fit curve as the early decay (i.e., within ≈100 seconds of write) rate as measured by V_T shift is either eratic or at a higher slope than the later portion of the plot. For this reason threshold measurements taken before and after normal military burn-in periods provide accurate data.

8.1.1 Static Retention Test Procedures

In investigating the Static Retention Parameter, several conditions of storage writing, erasing and device history should be measured and/or considered.

8.1.1.1 Writing

When attempting to make accelerated retention predictions the write and erasing conditions used to store the data should be well known and controlled to insure a "saturated" write condition has occurred. Devices that have been written or erased with less than adequate voltage or length of write will exhibit a reduced initial threshold window and may discharge at a different rate due to change in charge distribution. These conditions will cause reduced retention and will be difficult to correlate to other devices of the same or different types.

8.1.1.2 Temperature

The static retention behavior was studied under varied conditions of ambient temperature to determine its influence on the threshold level and decay rate. The +25^{o}C plot was used as a baseline.

8.1.1.3 Bias

The static retention condition was tested under conditions of no applied bias and nominal bias to determine the influence of applied bias on the threshold level and decay slope.

8.1.1.4 Device History

In making retention prediction comparisons between environmental and bias state conditions and unbiased room temperature retention, the results were compared against plots made at times close to those being compared to eliminate wear-out (endurance) effects and permanent shifts that may have resulted from the testing. In temperature testing data was taken both in the ascending and descending temperature directions to insure against thermal lag and permanent shifts due to the ambient.

Devices were also serialized and assigned to categories of testing to insure "worn-out" devices were not used to measure initial retention (i.e., devices segregated to performance testing, retention, endurance, D.C. parameters, etc.).

8.1.2 Results

Figures 8-2 through 8-5 show typical composite plots of each device type. These retention plots show the following:

a. +25^{o}C Ambient Retention (unbiased)

b. +125^{o}C Ambient Retention (unbiased)

c. Biased +25^{o}C Retention (using nominal specified bias)

d. +25^{o}C Ambient Retention (taken close to biased retention plot).

The plots show some interesting and unpredicted results:

a. High temperature ambient appears to cause an initial offset in the "0" threshold when the device was first placed in the oven that is permanent until rewritten. This shift would tend to cause reduced retention time prediction. In most cases however the initial retention remains ≥10 years. This problem was particularly noted on the single transistor per cell-devices (i.e., 2451 and 3400).

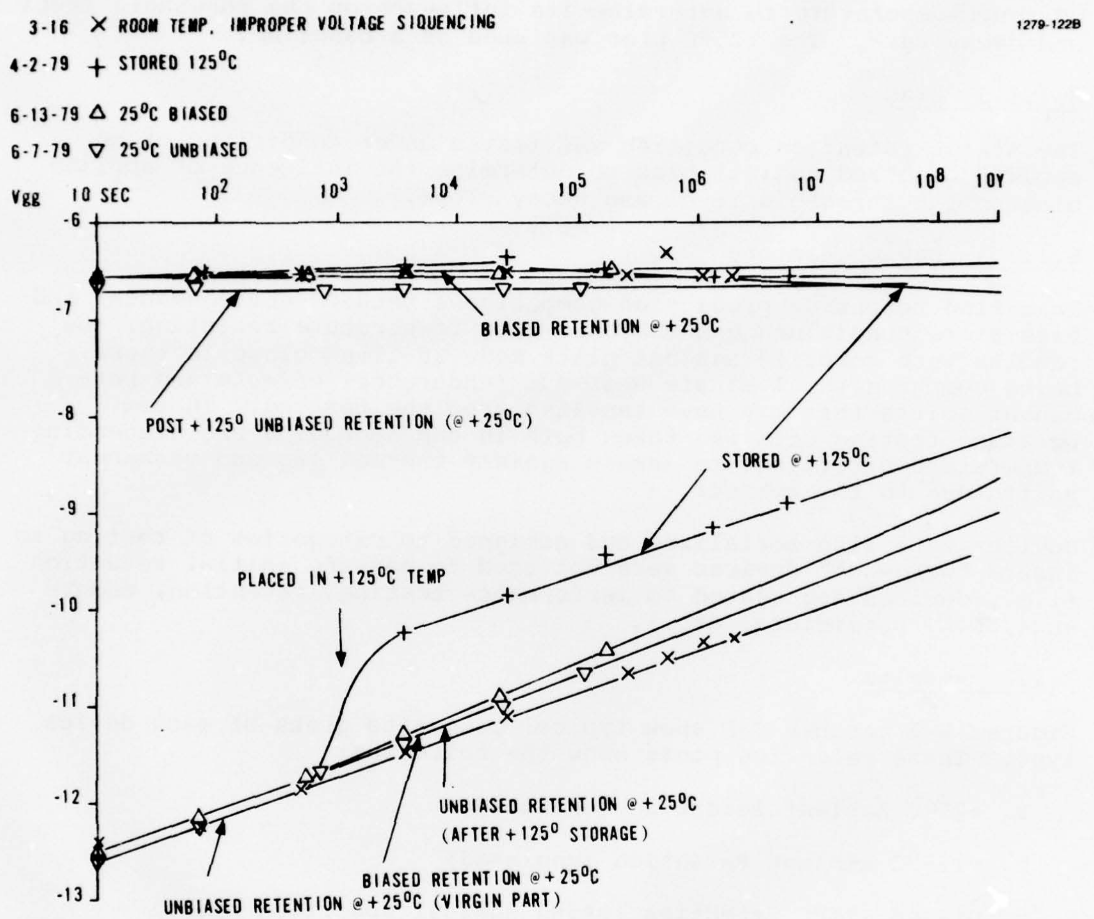

FIGURE 8-2. TYPICAL RETENTION PREDICTION PLOTS OF NCR2451

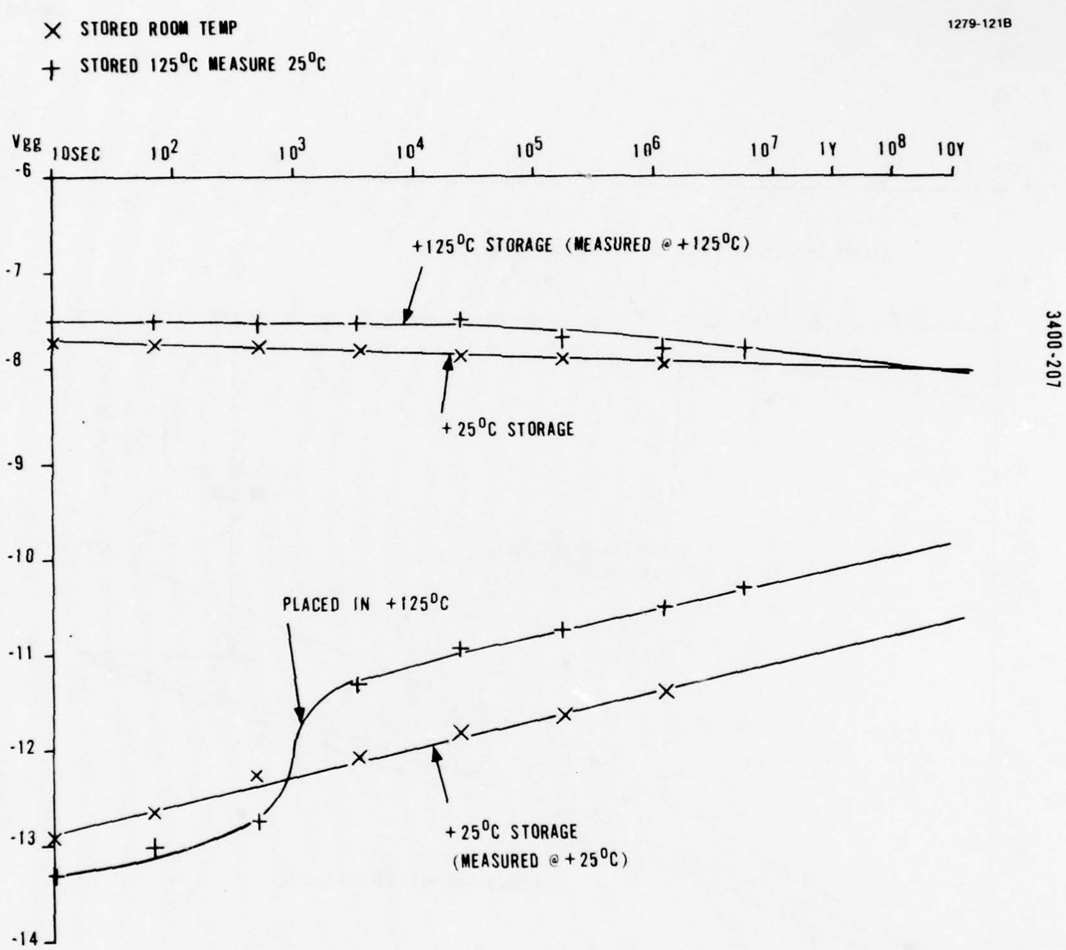

FIGURE 8-3. TYPICAL RETENTION PREDICTION PLOT FOR GI3400

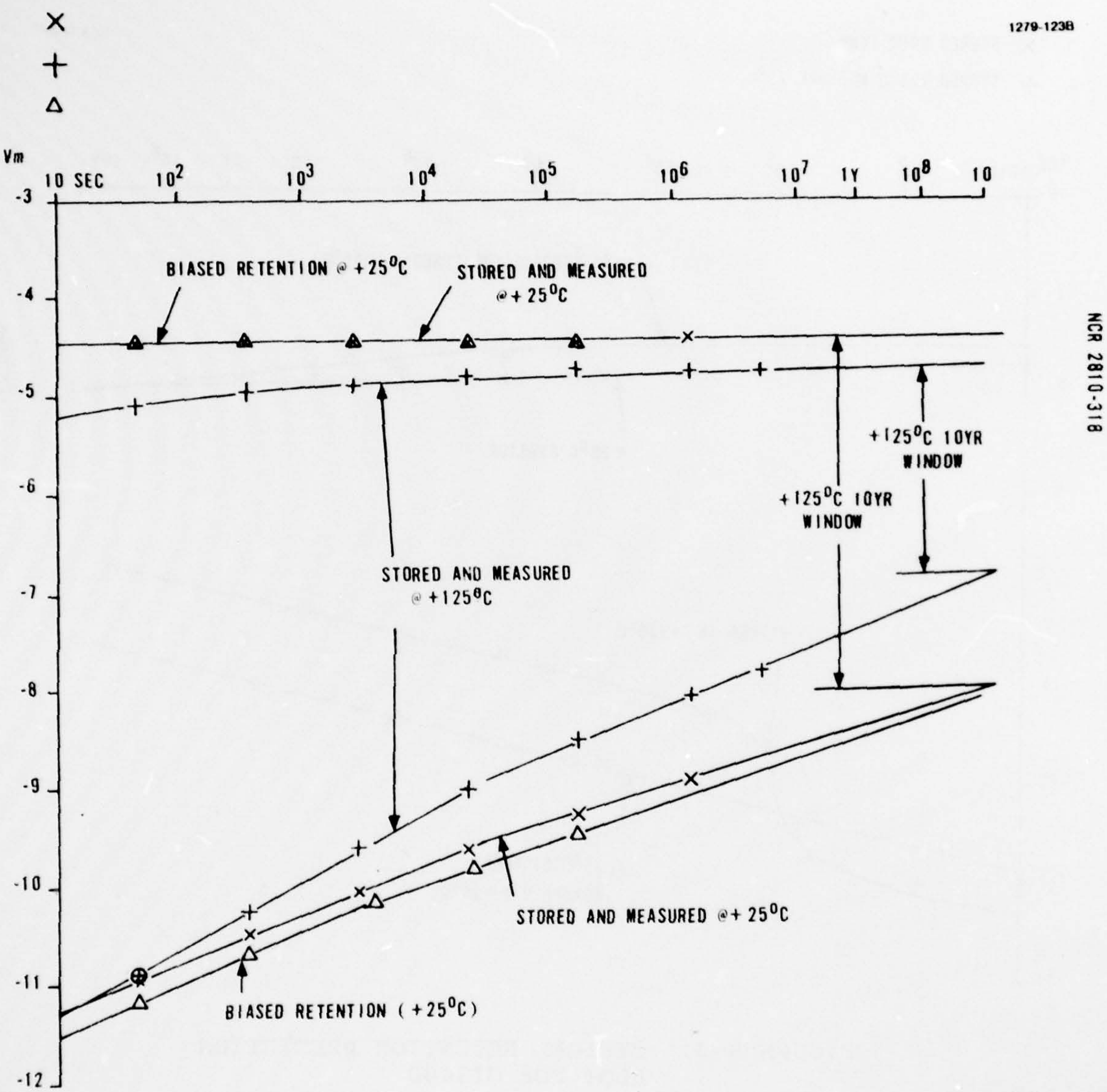

FIGURE 8-4. TYPICAL RETENTION PREDICTION PLOTS FOR NCR2810

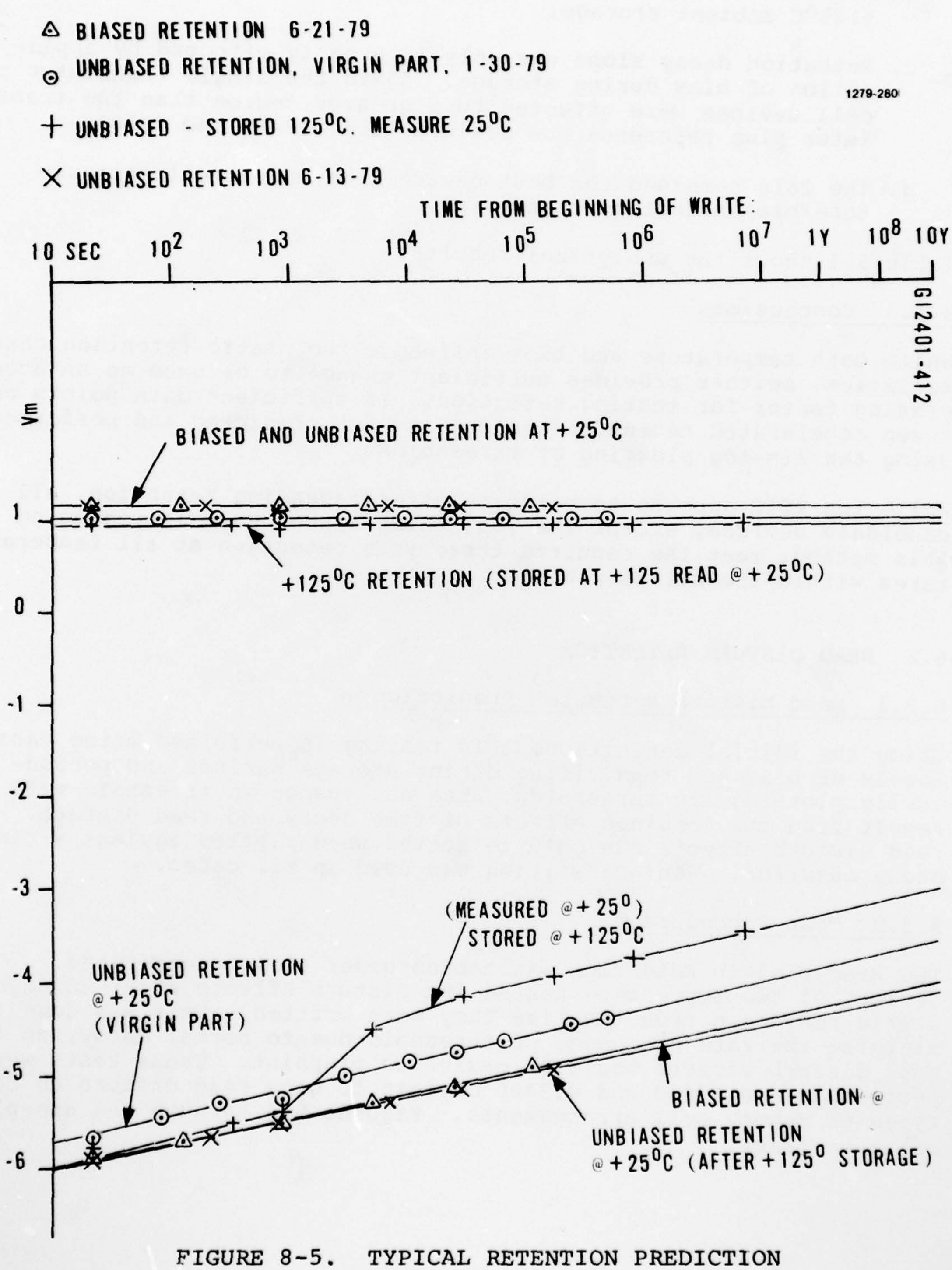

FIGURE 8-5. TYPICAL RETENTION PREDICTION PLOT FOR GI2401

b. Retention decay slope was not significantly affected by the +125°C ambient storage.

c. Retention decay slope was only marginally affected by application of bias during storage. Again the single transistor per cell devices were affected to a greater degree than the transistor plus reference row devices (i.e., 2401 and 2810).

d. The 2810 remained the best device from an overall temperature/bias retention standpoint.

Table 8-1 shows the analytical results.

8.1.3 Conclusions

While both temperature and bias influence the static retention characteristics, neither provides sufficient change to be used as an accelerating factor for testing retention. If sufficient data points are taken accelerated retention testing is best predicted and performed using the lin-log plotting of thresholds.

While the 2810 appears to perform better regarding retention, all candidate devices, except the 7053 which cannot be measured using this method, meet the required three year retention at all temperatures within the military range.

8.2 READ DISTURB RETENTION

8.2.1 Read Disturb Retention Prediction

Using the initial definition, this testing is performed using various levels of bias and read timing during storage periods and periodically plotting the thresholds. The net change in threshold will result from the combined effects of time decay and read disturb. The read disturb effects can only be sorted when plotted against a time decay baseline. Nominal writing was used in all cases.

8.2.2 Test Procedures

The Read Disturb Retention was tested under varied conditions. Devices of two types were tested for disturb effects after 28 days of static retention from the time they were written. This was done to minimize the rate of change of threshold due to normal decay, so that read disturb effects would be easier to pinpoint. These tests were performed on NCR2810 and GI3400 devices to show read disturb on both types of memory cell arrangements. Figures 8-6 through 8-8 are plots of this effect.

TABLE 8-1. RETENTION RESULTS

Device Serial	Initial Retention Cr Co*	Initial Retention Decay Rate	125°C Retention Cr Co*	125°C Retention Decay Rate	Off-Set at 10^3	After 125°C Retention Cr Co*	After 125°C Retention Decay Rate	Biased Retention Cr Co*	Biased Retention Decay Rate	Comments
2810										For 125°C test, devices written at temperature.
318	2.06×10^{12} -0.9979	-0.473	4.40×10^{9} -0.9988	-0.543	N/A	No Test		2.03×10^{12} -0.9975	-0.493	
319	1.98×10^{14} -0.9977	-0.382	1.07×10^{11} -0.9994	-0.442	N/A	No Test		7.36×10^{14} -0.9997	-0.376	
2401										Better retention after 125°C reflects a refinement of test procedure to minimize glitchs occurring at the initial-ization of MD-150 statewords.
412	4.74×10^{18} -0.9961	-0.299	1.02×10^{17} -0.9974	-0.293	0.843	1.48×10^{23} -0.9874	-0.255	9.55×10^{21} -0.9950	-0.269	
415	1.25×10^{18} -0.9771	-0.266	4.48×10^{12} -0.9946	-0.360	0.599	1.78×10^{19} -0.9993	-0.262	2.03×10^{20} -0.924	-0.248	
2451										Poorer retention after 125°C leads one to suspect a temperature related degradation of retention characteristic.
511	1.73×10^{10} -0.9976	-0.426	1.66×10^{7} -0.9999	-0.447	1.278	3.75×10^{9} -0.9996	-0.463	8.28×10^{8} -0.9987	-0.503	
513	3.95×10^{10} -0.9999	-0.445	1.76×10^{8} -0.9957	-0.376	1.413	8.41×10^{9} -0.9994	-0.462	1.66×10^{9} -0.9991	-0.505	
3400										
207	1.15×10^{11} -0.9976	-0.309	3.08×10^{8} -0.9940	-0.297	1.232	No Test		No Test		Reference Voltage: -9.44 Decay at 125°C
2.09	1.17×10^{10} -0.9966	-0.353	1.16×10^{8} -0.9901	-0.305	1.298	No Test		No Test		Reference Voltage: -9.90

*Cr Co - Correlation Coefficient

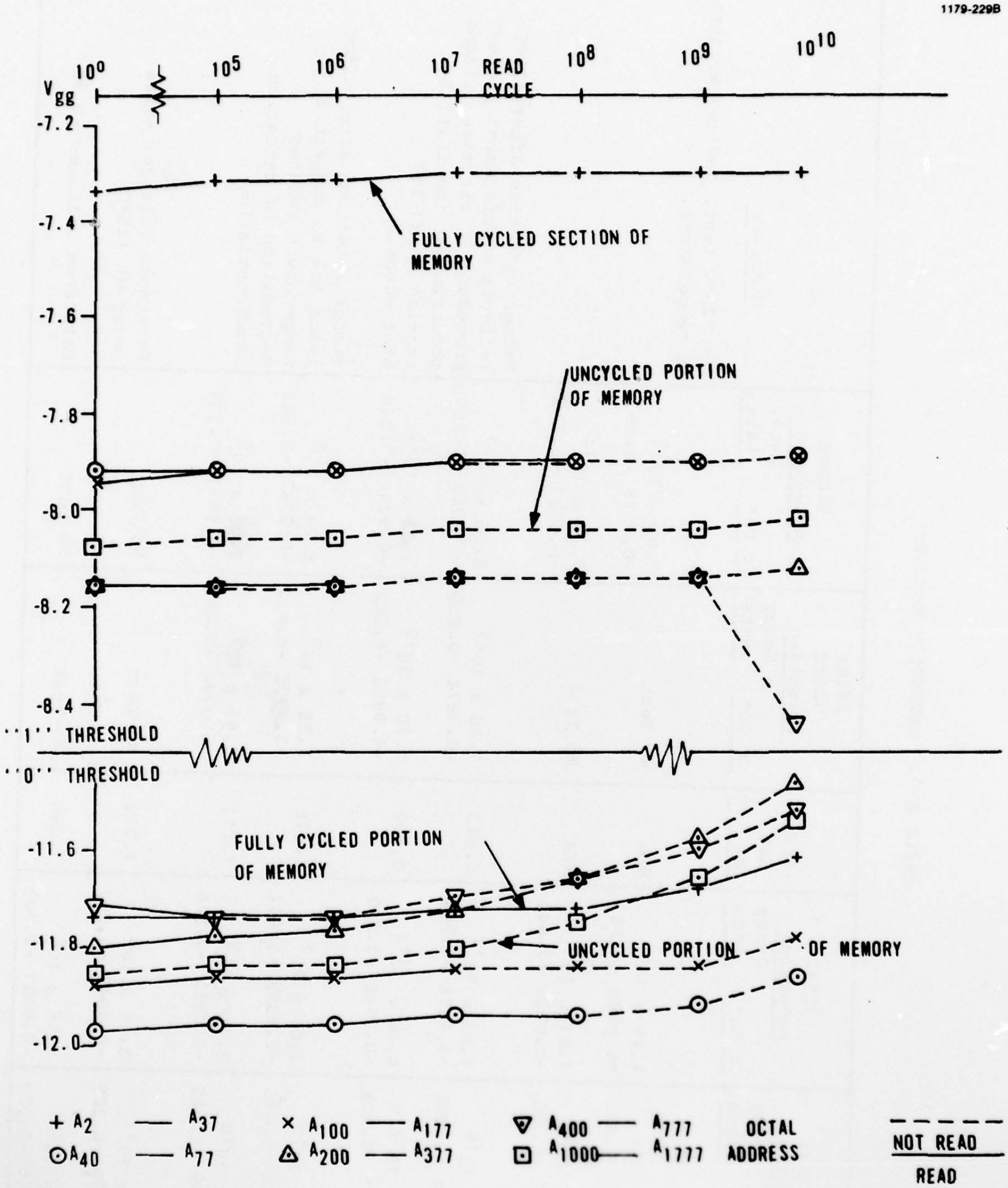

FIGURE 8-6. READ DISTURB RETENTION ON GI 3400 AFTER 28 DAYS OF STORAGE AT +25°C

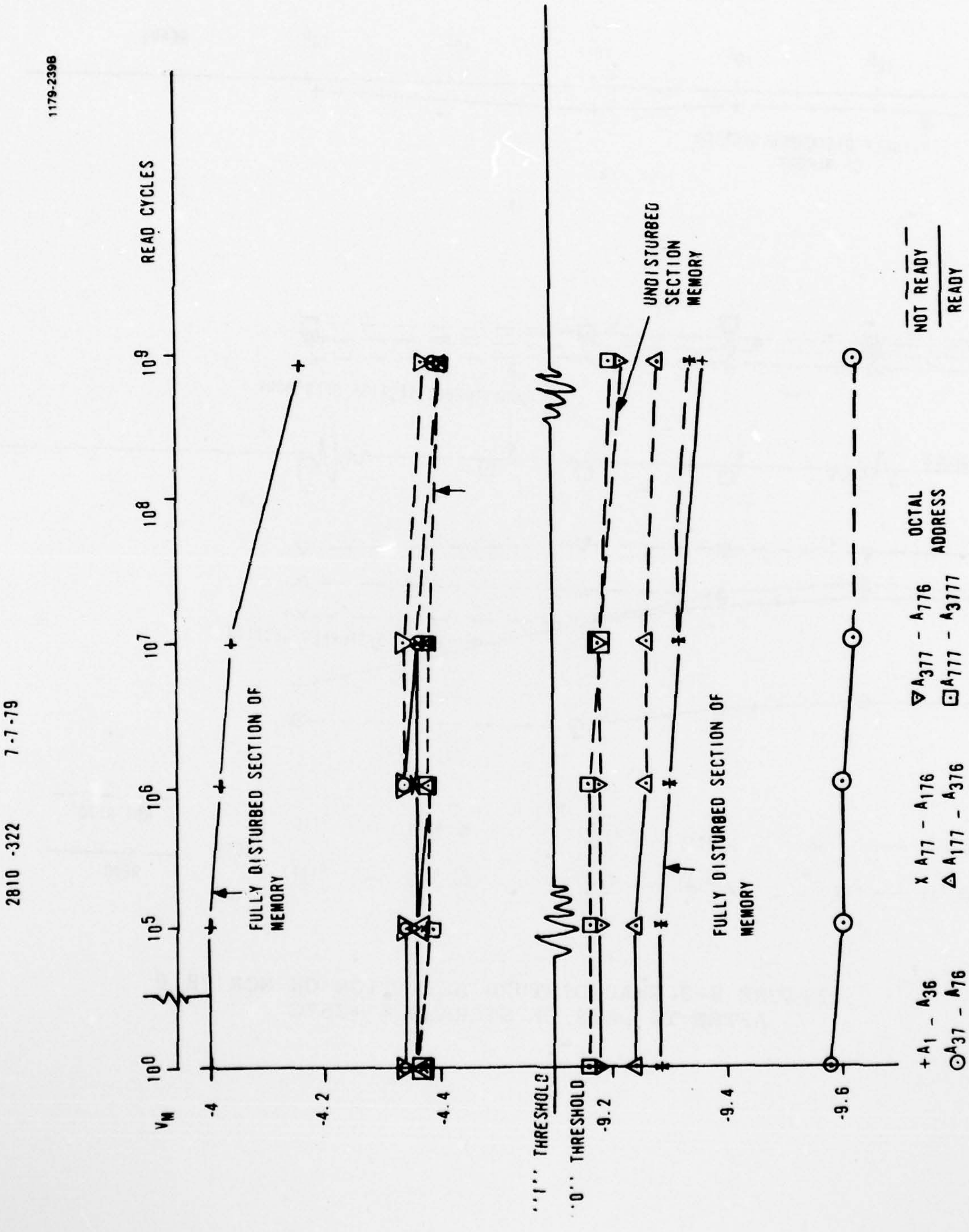

FIGURE 8-7. READ DISTURB RETENTION ON NCR2810 AFTER 109 DAYS OF STORAGE @ +25°C

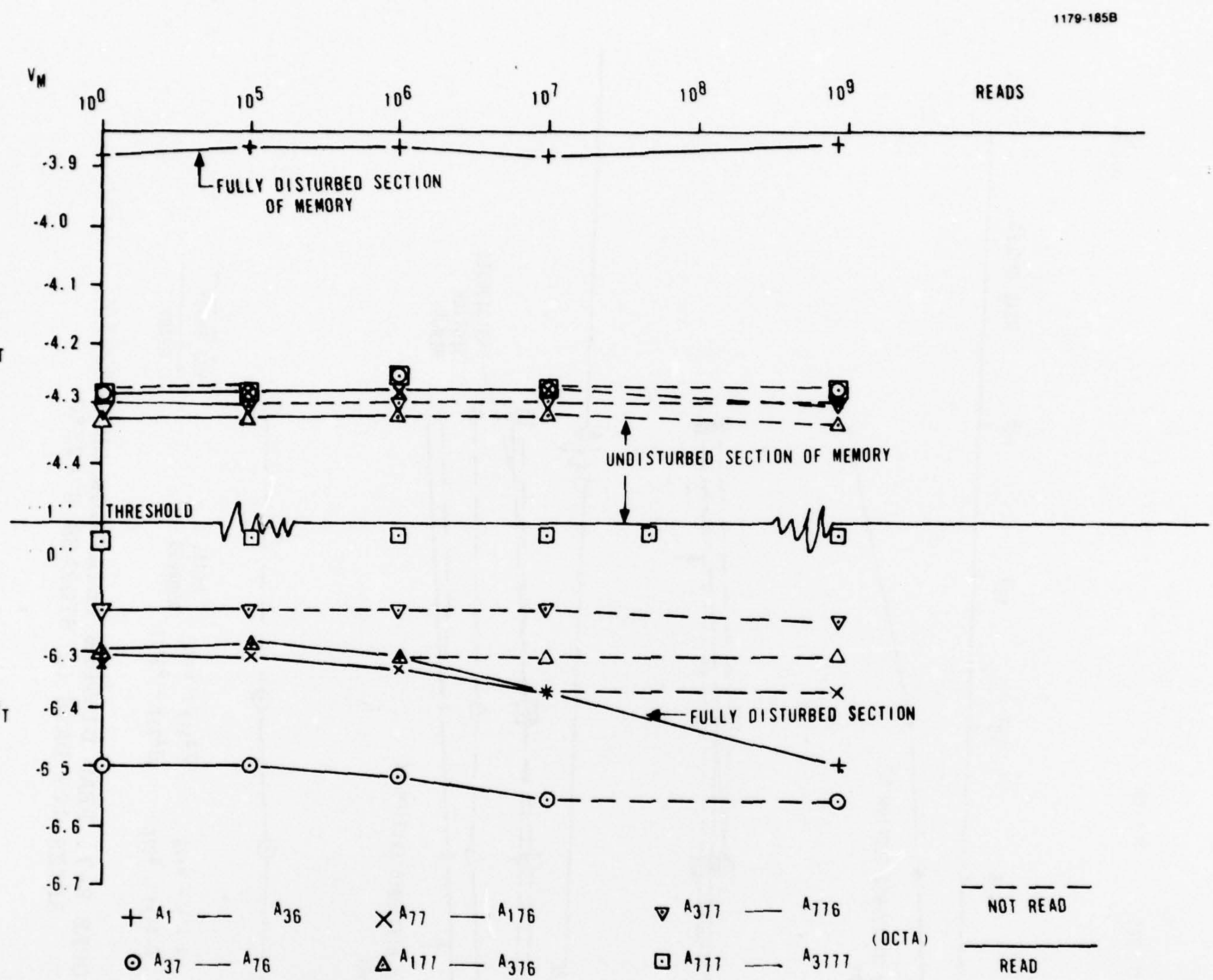

FIGURE 8-8. READ DISTURB RETENTION ON NCR 2810
AFTER 24 DAYS OF STORAGE @ +25°C

To determine the effect of read disturb on newly written devices the NCR2451 and GI2401 were written and then immediately read cycled. The effects are shown in Figures 8-9 through 8-11. Figure 8-11 shows the read disturb effects on retention after 10^5 erase/write cycles.

8.2.3 Results

The results show that read cycling has the following effects:

a. For the single transistor/cell devices (i.e., 2451 and 3400) read cycling enhances the "0" threshold while having only small effects on the "1" threshold. The net effect is to expand the sense window and increase retention.

b. For the transistor plus reference row devices (i.e., 2401 and 2810) the "0" threshold is reinforced while the "1" threshold is disturbed due to read cycling. It appears that the longer the storage time the more effect read cycling has on the "1" threshold, the net effect of read cycling on these devices is to maintain the sense window more stable than in static retention.

c. High E/W cycling results in increased effect on the "1" threshold with little change in the effect on the "0" threshold of read cycling on the latter type devices.

8.2.4 Conclusions

Read cycling has varied effects on the retention of MNOS devices with the general effect being one of reducing decay of the "0" threshold and increasing decay of the "1" threshold. While continuous read cycling will cause threshold decay to the point of failure to sense the stored state, it works in opposition to time decay. Stored ones will fail as a result of read cycling while in general zeros will eventually fail for time decay retention cases. No apparent advantage is shown for any candidate device with the 2401 being little affected by read disturb and the 2810 being reinforced by this testing.

8.3 ENDURANCE

8.3.1 Background

Earlier in this report, endurance was defined as the change of retention of MNOS memory device (or other nonvolatile memory device) for a fixed number of write/erase cycles. Once a device has experienced a large number of E/W cycles the degraded retention performance is not correctable by feasible means and thus represents a permanent shift.

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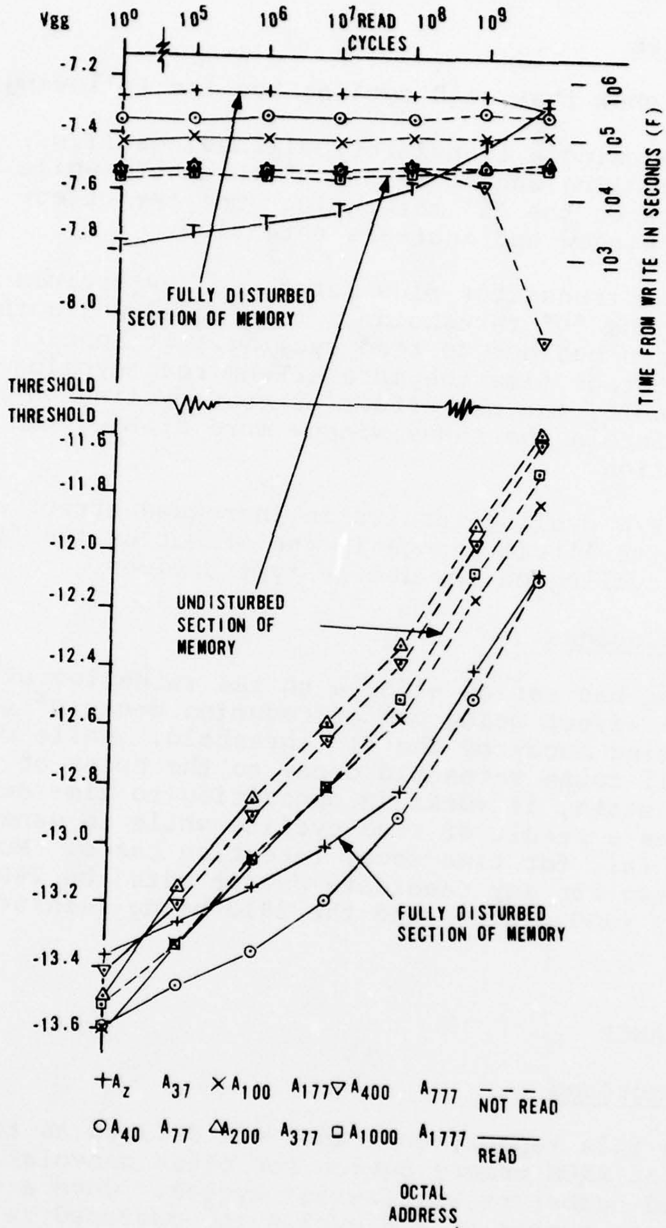

FIGURE 8-9. READ DISTURB RETENTION OF NCR-2451
(Immediately after Write)

1279-124B

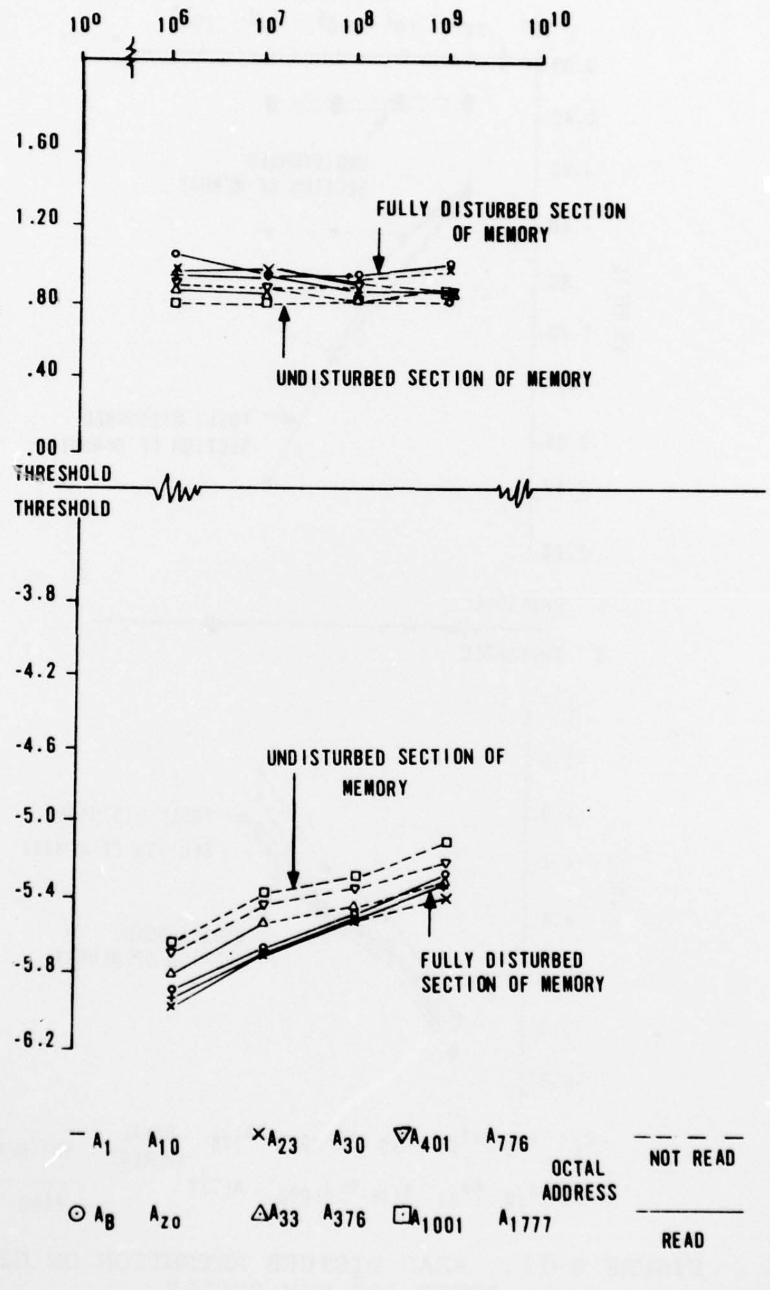

FIGURE 8-10. READ DISTURB RETENTION OF GI2401
(Immediately after Write)

1279-125B

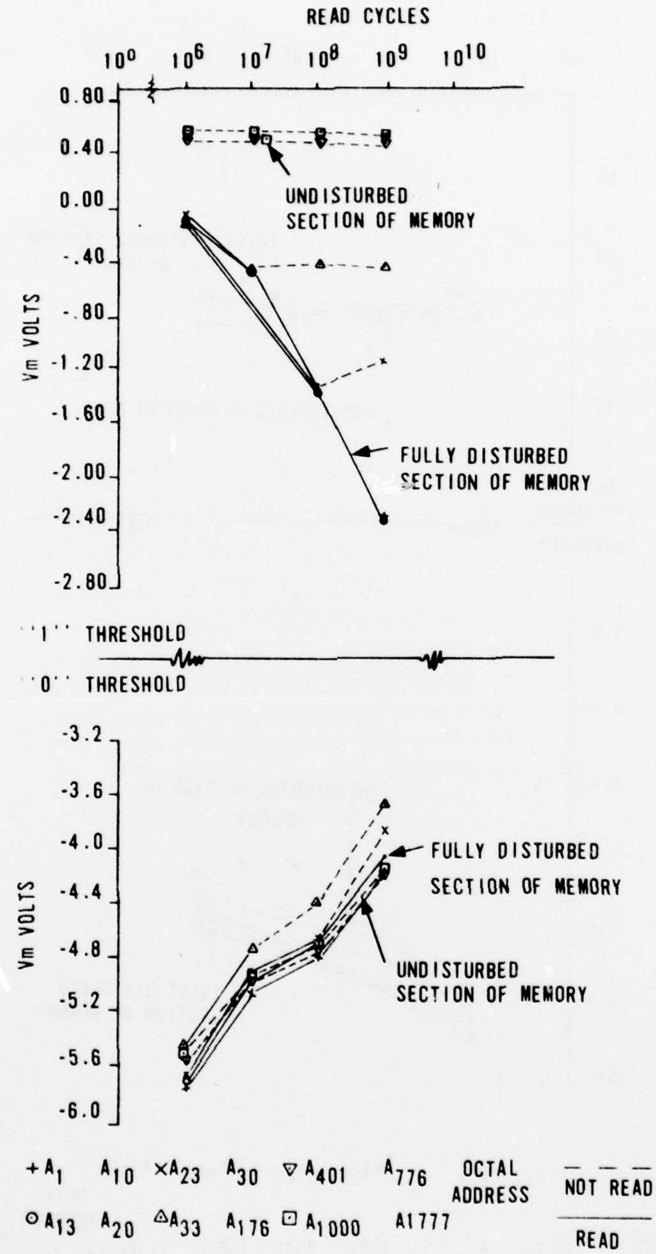

FIGURE 8-11. READ DISTURB RETENTION ON GI2401 AFTER 10^5 E/W CYCLES

Previous methods of screening devices were therefore limited to lot sampling some devices and performing destructive E/W cycling. The endurance of the lot was then gauged by the performance of the sample devices. This method was only marginally successful since the endurance of devices in the same lot varied widely. Only gross sorting was accomplished since devices made under the same process control at the same time tended to produce a distribution of endurance, the center of which shifted on a lot basis.

In cooperation with NCR personnel, the relationship between nitride thickness and endurance was investigated to determine if a practical screening method could be devised. Since endurance testing was necessary to fulfill MACI requirements, a data base that could be used to establish the nitride thickness/endurance correlation would be established.

Since the device nitride thickness was measured by NCR using the voltage necessary to cause a specified current between two internal pads on the chip (not connected to the external package pins), this method was not practical to a potential device user (for details of their method see NCR). It was then suggested that hard-writing a device to an all zero's mode and soft erasing with either reduced erase voltage or time would produce a threshold shift that was a function of the nitride thickness. Since it is known that the erasing rate is a function of the nitride thickness, some tests using this phenomenon were devised.

By first writing a device using nominal specifications into an all-zero pattern and erasing the device using reduced erase voltages and shortened erase time, the conditions for measuring relative nitride thickness are created. The device "0" (minimum) thresholds (V_T) were measured following the soft-erase and recorded. Devices having thinner nitrides will erase faster and at lower potentials thereby resulting in more positive (re: lower V_T) values of the minimum "0" V_T's. By grading devices by the minimum post-soft erase "0" V_T an order of relative nitride thickness of devices can be established. With sufficient data base a correlation between this measured threshold and device endurance can be established.

To establish an alternate test that would apply to devices which did not have threshold measurement capabilities another test was developed. By hard writing zeros first, then alternately performing soft erases and reading the device output for a switch from zeros to ones, a measure of nitride thickness could be made. The larger the number of soft-erase/read cycles it required to produce the first switch to a "1" state, the thicker the nitride. In other words, devices that switched with one or a few erase/read cycles were considered thin nitride devices. The devices were then graded by increasing number of erase/read cycles as thicker nitride parts.

Device samples from various positions in both these gradiations were selected for endurance testing and the results compared to their relative position in the graded lists. As will be shown, there was general correlation between high endurance parts and listed thicker nitrides.

When developed with greater data base, this testing could create a nondestructive screening method that could be used with 100 percent testing to eliminate a high percentage of low endurance parts that otherwise would be impractical to identify. An additional feature is that the testing method integrates easily into normal parameter and retention testing and does not require long testing periods.

8.3.2 Test Procedures

8.3.2.1 Endurance Screening

The methods were discussed in the previous section.

The "V_m" method of measuring thresholds is used (see Attachment D). By using this method, similar methods are used for both single transistor/cell and transistor plus reference row/cell devices. Other methods developed by NCR use the "V_R" method of V_T measurement. (See NCR for details).

8.3.2.2 Endurance Measurement

The actual endurance of selected devices of each type was measured by write/erase cycling the devices, using all zeros in the writing, and periodically performing two-day retention plots. These plots were made after the following number of E/W cycles; 10^4; 3 x 10^4, 7 x 10^4 and 10^5. The plots were made on the same lin-log graph paper for each device to illustrate the shift in retention. Best fit curves were developed for each retention plot and then extended until the one and/or zero curves met the end of life criteria mentioned in subsection 8.1 for each respective device type. These criteria were set at the maximum values for that device type and are therefore conservative. This results in values being minimum retention for each device type.

8.3.3 Results

Due to the complexity of this parameter the results on the endurance testing and predictive screening is given completely for each device.

8.3.3.1 NCR2451

Table 8-2 provides the analyzed data taken on the 2451 devices ordered for MACI (new thick nitride parts were later received and are under test). This table provides the number of the device tested,

TABLE 8-2. ENDURANCE DATA FOR NCR 2451

Device	Reference Voltage	E/W Cycles	0 Bound Erased at Vgg=-18V	16V Erases to Fail	Threshold Window at 10 seconds	Slope For 0 Bound (Written State) Volts/Decade			Slope 1 Bound Volts/Decade			Normalized Retention at 0.35 Volts Offset From Reference Volt	Correlation Coefficient -1=linear
						Ave	Max	Min	Ave	Max	Min		
518 X	-9.43	10^0	-9.16	4	13.60	0.488	0.873	0.094	-0.134	0.023	-0.424	3.87×10^{10}	-0.9514
		10^4			13.30	0.740	1.37	0.467	-0.002	0.016	-0.024	2.03×10^6	-0.9941
		3×10^4			13.44	0.764	0.841	0.664	0	0.024	-0.023	5.35×10^5	-0.9994
		7×10^4			13.28	0.903	0.991	0.802	0.019	0.024	0	7.15×10^4	-0.9997
		10^5			13.26	0.963	1.03	0.850	0.014	0.070	-0.024	4.03×10^4	-0.9997
519 △	-9.43	10^0	-8.84	2	---	0.503	0.590	0.448	0	0.074	-0.071	1.09×10^{10}	-0.9987
		10^4			13.96	0.716	1.24	0.377	0.003	0.067	-0.075	3.19×10^6	-0.9916
		3×10^4			13.74	0.864	0.920	0.802	0.009	0.023	0	3.55×10^5	-0.9998
		7×10^4			13.62	0.976	1.04	0.869	0.009	0.069	-0.048	7.65×10^4	-0.9997
		10^5			13.46	1.00	1.11	0.826	0.14	0.024	0	4.65×10^4	-0.9994
520 ▽	-9.24	10^0	-7.82	1	13.3	0.401	0.469	0.333	0	0.047	-0.071	1.11×10^{10}	-0.9989
		10^4			13.18	0.741	0.755	0.708	0.009	0.024	-0.024	6.52×10^5	-0.99992
		3×10^4			12.90	0.812	0.897	0.650	0.009	0.024	-0.024	9.69×10^4	-0.99913
		7×10^4			12.98	0.996	1.05	0.902	0.009	0.071	-0.025	2.38×10^4	-0.99980
		10^5			12.80								
522 ○	-9.54	10^0	-8.82	2	13.8	0.628	1.23	0.334	0.005	0.024	-0.024	3.14×10^9	---
		10^4			13.8	0.732	1.23	0.354	0	0.024	-0.024	2.45×10^6	-0.9866
		3×10^4			13.6	0.807	0.856	0.708	0.009	0.035	0	3.94×10^5	-0.9997
		7×10^4			13.68	0.943	1.01	0.845	0.009	0.046	-0.024	9.53×10^4	-0.9997
		10^5			13.58	0.991	1.07	0.892	0.013	0.044	0	5.36×10^4	-0.9997
523 □	-9.40	10^0	-8.96	2	---	0.527	0.826	0.354	-0.016	0.024	0	4.94×10^9	-0.9782
		10^4			14.3	0.732	0.779	0.708	0.009	0.024	0.024	1.60×10^7	-0.9993
		3×10^4			14.14	0.873	0.920	0.826	0.009	0.024	0	1.05×10^5	-0.99988
		7×10^4			13.96	1.03	1.11	0.873	0.019	0.024	0	1.25×10^5	-0.9994
		10^5			13.78	1.05	1.18	0.899	0.014	0.046	-0.024	7.18×10^4	-0.9989

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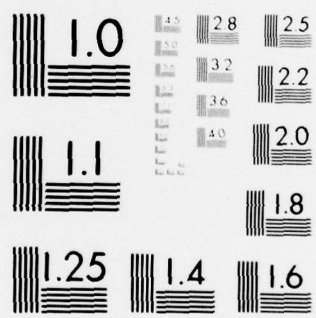
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its internal reference voltage, the number of E/W cycles it was exposed to, the soft erase V_T (0 Boundry), the number of soft erase cycles until "0" fail, 10 second V_T window, the "0" V_T curve slope, "1" V_T curve slope, the predicted retention using the estimated best fit curve and the curve correlation coefficient to the data. This data is provided for all five sample devices used for endurance testing.

These results show that while every device meets the three-year retention requirement of MACI initially, all would fail that criteria after 10^4 E/W cycles. Figures 8-12 and 8-13 are endurance plots of selected 2451 devices.

The histograms shown in Figure 8-14 are plots of the distribution of the soft erase V_T's (a) and the required number of soft erases to switch from "0" to "1" of first cell (hereafter known as Endurance Prediction Test 1 and 2, respectively) for all of the original 2451 devices. The endurance (V_T window closure @ $3x10^4$ E/W cycles) is plotted on both histograms using the scale between them. These composite plots show the relationship between the predictive criteria and the endurance of the devices. The lower endurance parts tend to require less soft erase cycles and exhibit lower soft erase V_T than their higher endurance parts. Since the predictive techniques are more restricted with parts like the NCR2451 and GI3400 which have on-chip voltage regulators, the correlation is less clear.

Figure 8-15 plots the retention of the selected 2451 parts against the number of E/W cycles. The predictive data is listed on the individual curves and shows the correlation to the endurance of the devices.

<u>8.3.3.2 GI3400</u>

Table 8-3 is the equivalent of Table 8-2 for the GI3400. This table shows the endurance data for the selected 3400 devices. The data indicated general agreement with both predictive tests with regard to endurance correlation. On both Tables 8-2 and 8-3 the increased slope of the "0" retention curve indicates the endurance effect. It is noteworthy that the"1" slope does not change with E/W cycling.

Figures 8-15 and 8-16 show endurance plots of relatively thick and thin nitride devices, respectively. The plots show higher endurance for the thicker part. These plots also point out that while each device would meet MACI retention requirements initially that neither would qualify after 10^4 E/W cycles. One of the tested devices (#212) would meet the three-year retention @ 10^4 E/W cycles (See Table 8-3).

TABLE 8-3. ENDURANCE DATA FOR GI 3400

Device	Reference Voltage	E/W Cycles	0 Bound Erased at Vgg=-18V	16V Erases to Fail	Threshold Window at 10 seconds	Slope For 0 Bound (Written State) Volts/Decade			Slope 1 Bound Volts/Decade			Normalized Retention at 0.35 Volts Offset	Correlation Coefficient -1=linear
						Ave	Max	Min	Ave	Max	Min		
215 ○	-9.62	10^0	-9.81	4	13.46	0.373	0.401	0.350	0	0.024	-0.047	2.15×10^{10}	-0.9997
		10^4			13.60	0.639	0.700	0.566	0.009	0.036	0	3.76×10^6	-0.9994
		3×10^4			13.66	0.816	0.929	0.684	-0.009	0	-0.041	3.82×10^6	-0.9987
		7×10^4			13.46	0.956	1.04	0.744	-0.005	0	-0.024	5.11×10^4	-0.9988
		10^5			13.56	0.987	1.16	0.802	-0.014	0	-0.071	5.04×10^4	-0.9984
213 □	-9.7	10^0	-9.7	8	13.68	0.378	0.543	0.256	-0.004	0.165	-0.094	2.24×10^{10}	-0.9961
		10^4			13.86	0.593	0.706	0.486	0.006	0.024	0	2.11×10^7	-0.9980
		3×10^4			13.86	0.778	0.875	0.661	-0.001	0.067	-0.075	8.08×10^5	-0.9991
		7×10^4			13.68	0.908	1.01	0.684	-0.004	0.095	-0.093	1.12×10^5	-0.9987
		10^5			13.82	0.968	1.11	0.779	0	0.048	-0.048	8.94×10^4	-0.9987
212 ◇	-9.62	10^0	-11.09	27	13.12	0.326	0.448	0.203	-0.033	0	-0.047	2.88×10^{10}	-0.9963
		10^4			13.94	0.525	0.563	0.484	-0.011	0.212	-0.269	3.86×10^8	-0.9998
		3×10^4			13.9	0.640	0.706	0.566	-0.006	0.028	-0.061	1.68×10^7	-0.9994
		7×10^4			13.96	0.770	0.893	0.597	0.060	0.231	0	1.75×10^6	-0.9978
		10^5			13.9	0.812	0.959	0.519	0.009	0.070	-0.048	8.22×10^5	-0.9962
214 △	-9.74	10^0	-10.02	4	13.44	0.378	0.472	0.256	-0.009	0.165	-0.186	5.94×10^9	-0.9965
		10^4			13.56	0.562	0.616	0.472	-0.014	0	-0.047	1.60×10^7	-0.9990
		3×10^4			13.36	0.715	0.833	0.613	-0.017	0.026	-0.047	4.31×10^5	-0.9990
		7×10^4			13.44	0.705	0.990	0.472	0	0.024	-0.024	1.70×10^5	-0.9970
		10^5			13.50	0.754	1.05	0.202	-0.005	0.023	-0.48	1.65×10^5	-0.9926
227 ▽	-9.91	10^0	-9.58	3	13.64	0.397	0.478	0.350	0.005	0.048	-0.047	4.87×10^9	-0.9992
		10^4			13.84	0.657	0.732	0.519	-0.005	0.047	-0.075	3.23×10^6	-0.9983
		3×10^4			13.64	0.823	0.943	0.684	-0.023	0	-0.047	1.53×10^5	-0.9987
		7×10^4			13.80	0.988	1.09	0.802	0.005	0.070	-0.047	4.59×10^4	-0.9989
		10^5			13.70	1.01	1.18	0.779	-0.019	0	-0.047	3.06×10^4	-0.9980
205 X	-9.54	10^0	-9.67	4	13.36	0.378	0.448	0.030	0	0.024	-0.024	1.34×10^{10}	-0.9987
		10^4			13.42	0.614	0.684	0.496	0	0.047	-0.024	6.31×10^6	-0.9988
		3×10^4			13.28	0.759	0.854	0.614	-0.011	0.028	-0.060	3.8×10^5	-0.9984
		7×10^4			13.44	0.918	1.10	0.684	0	0.096	-0.093	8.75×10^4	-0.9978
		10^5			13.46	0.967	1.12	0.755	0	0.024	0.048	5.67×10^4	-0.9983

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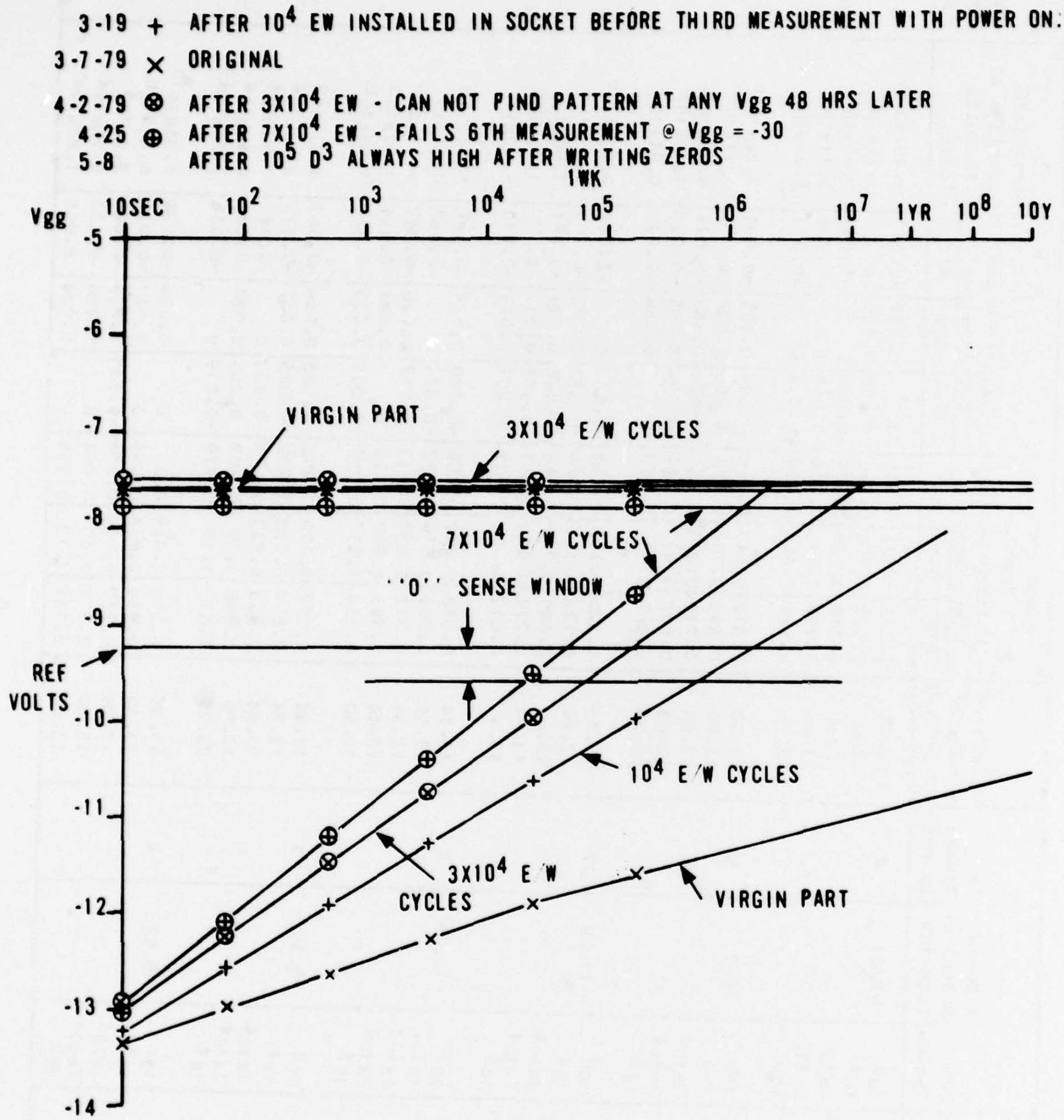

FIGURE 8-12. ENDURANCE PLOT OF
NCR 2451 (RELATIVELY THIN NITRIDE DEVICE)

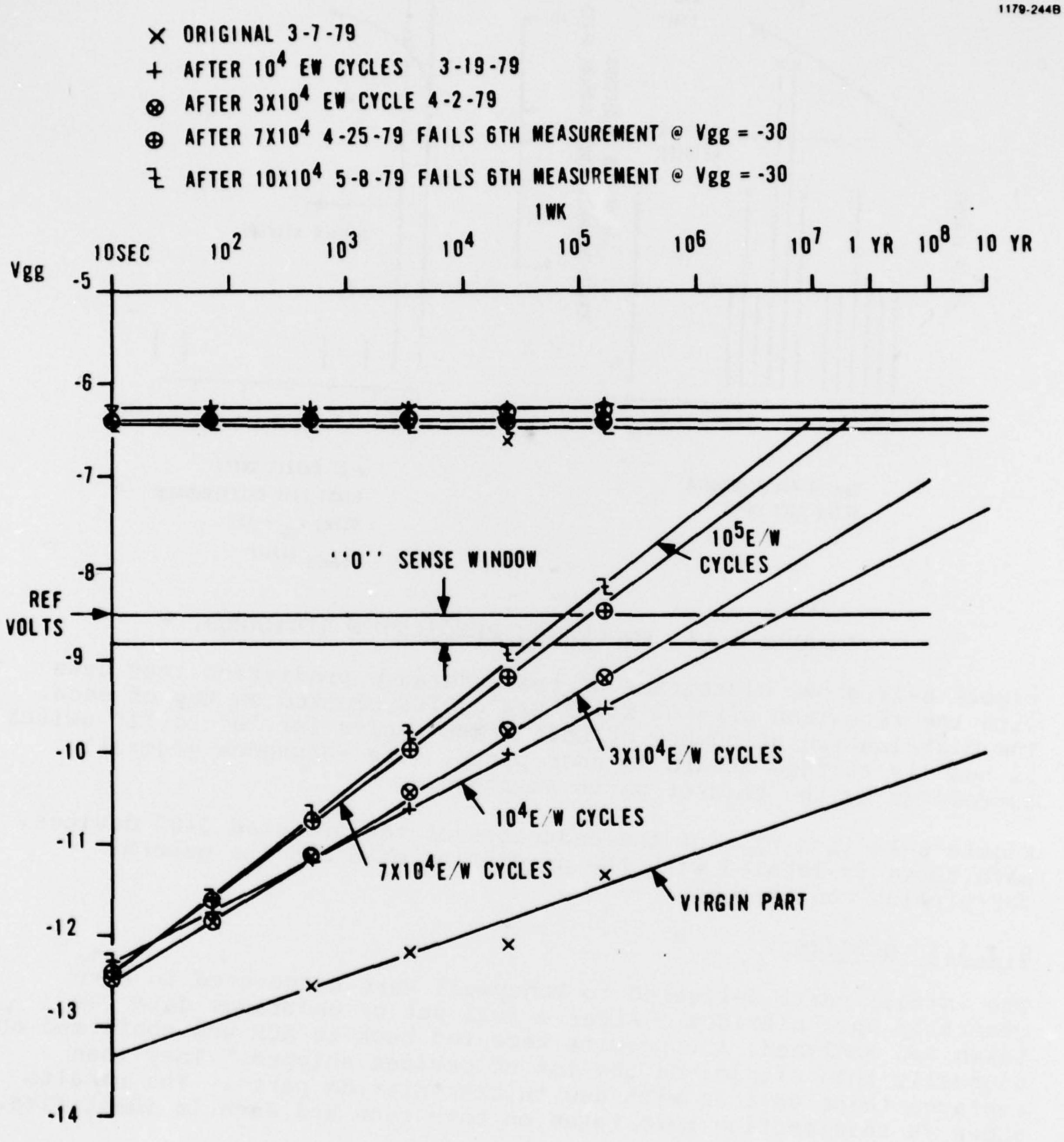

FIGURE 8-13. ENDURANCE PLOT OF
NCR 2451 (RELATIVELY THICK NITRIDE)

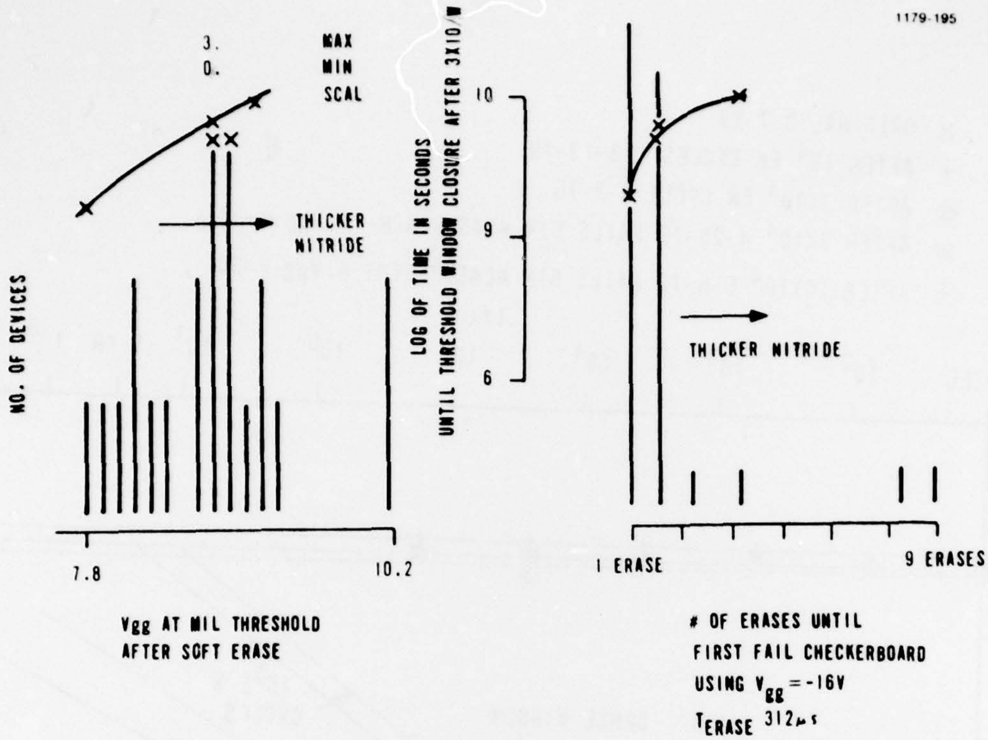

FIGURE 8-14. ENDURANCE PREDICTION HISTOGRAM

Figure 8-17 shows histograms of the endurance prediction test data with the retention after 3 x 10^4 E/W cycles plotted on top of each. The distribution of number of soft erase cycles for "0" to "1" switch is heavily shifted toward thinner parts. The endurance generally correlates to the thicker parts as shown.

Figure 8-18 is a plot of the endurance of the selected 3400 devices. Each curve is labeled with the predictive data and the general correlation can be seen.

8.3.3.3 NCR2810

The initial parts delivered to Honeywell were discovered to have generally thin nitrides. After a full set of endurance data was taken and analyzed, the results were fed back to NCR who confirmed an unusually thin nitride on the lot of devices shipped. They then replaced these devices with new thicker nitride parts. The results shown in this section were taken on both runs and each is identified.

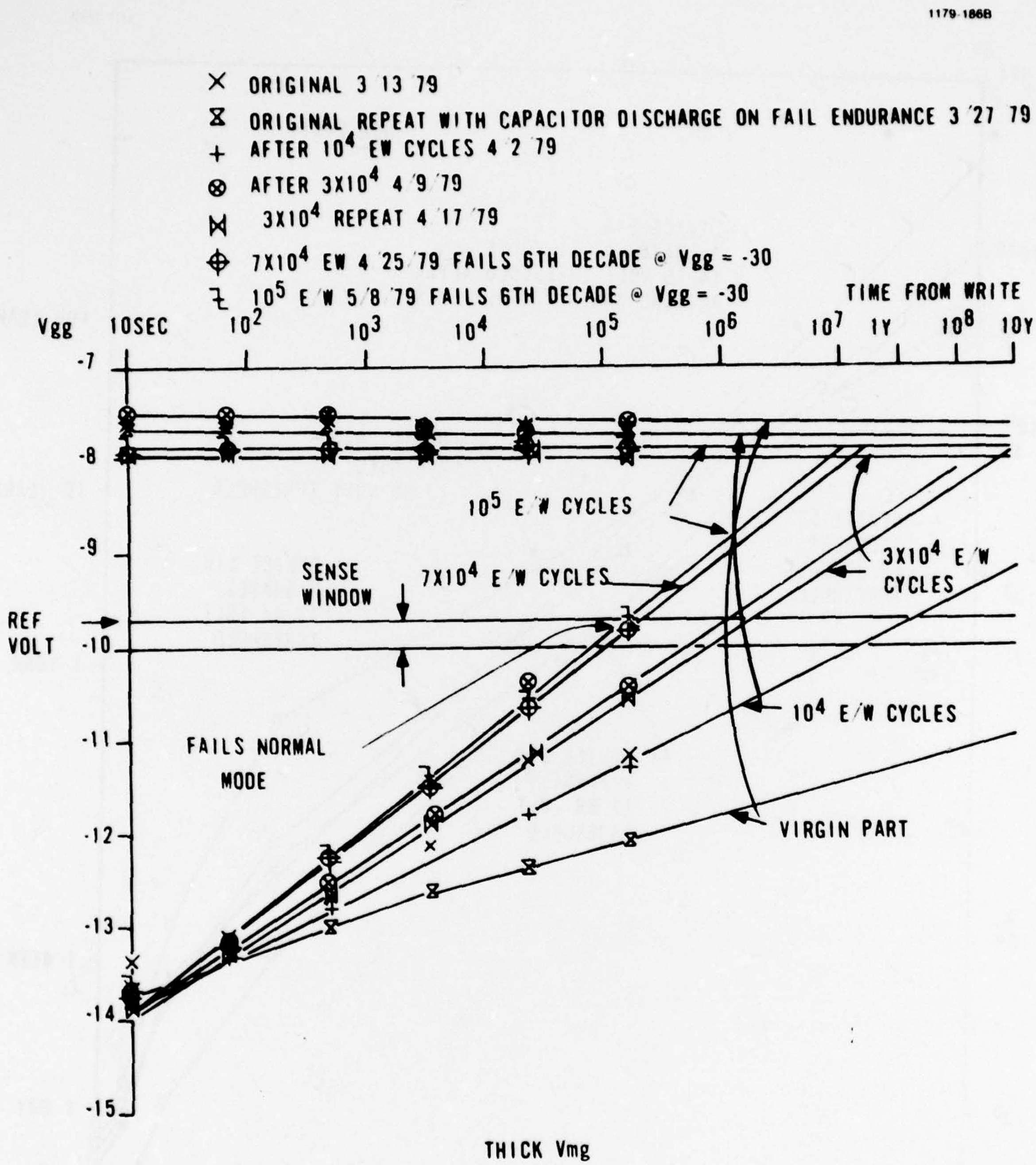

FIGURE 8-15. ENDURANCE OF
NCR 2451 (RETENTION VS AND ERASE/WRITE CYCLES)

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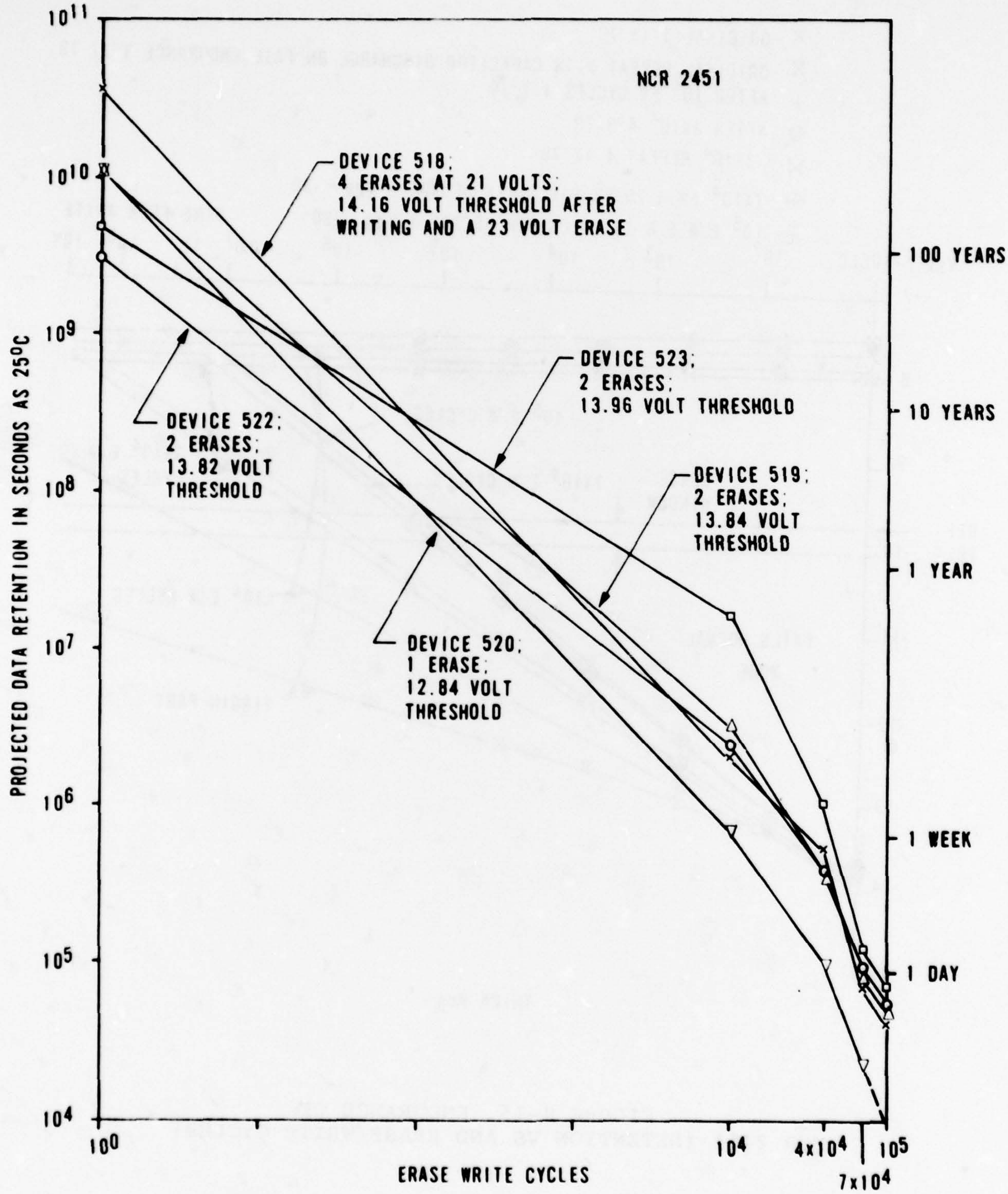

FIGURE 8-15. ENDURANCE OF
NCR 2451 (RETENTION VS AND ERASE/WRITE CYCLES) (Cont)

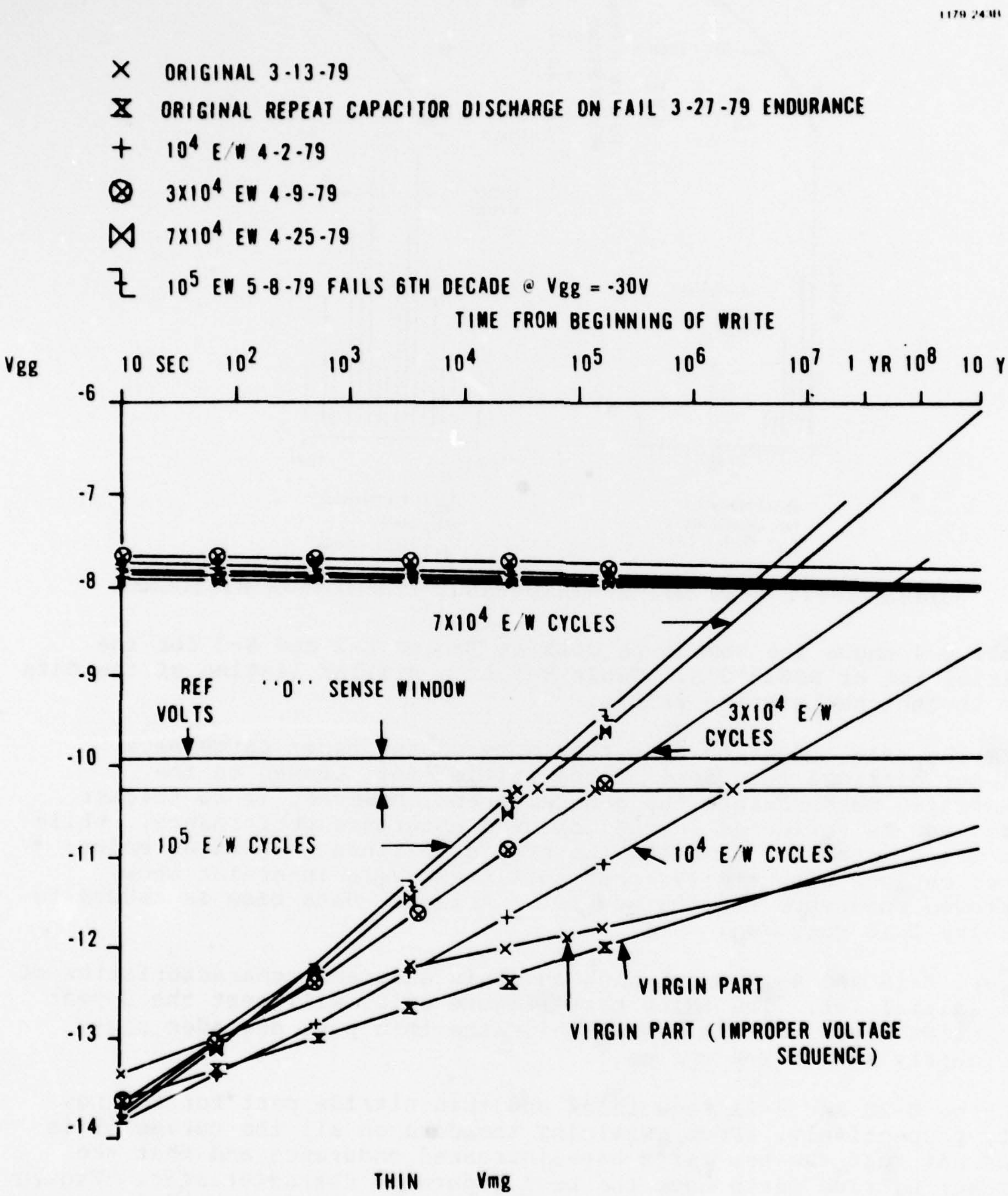

FIGURE 8-16. ENDURANCE OF GI 3400 (RELATIVELY THIN NITRIDE)

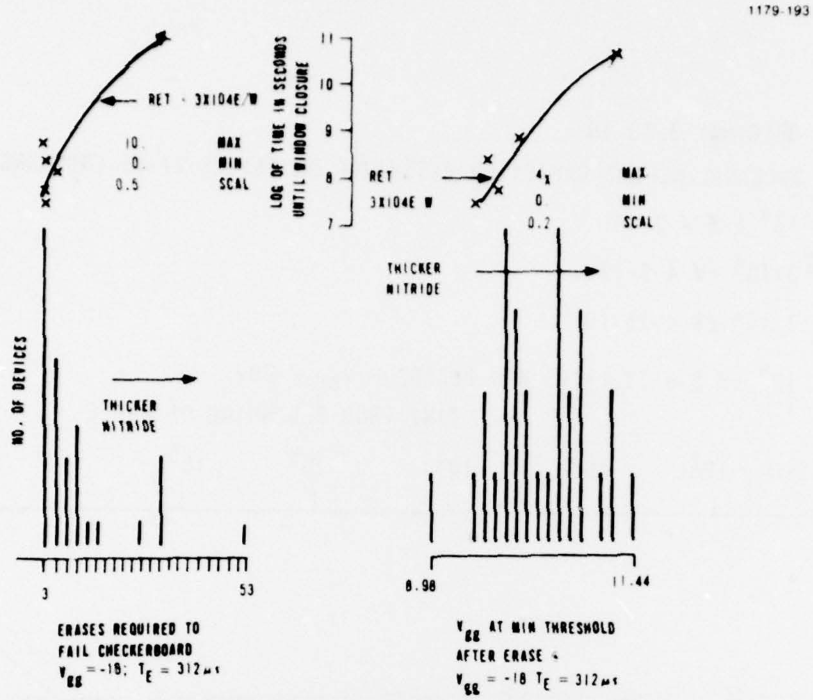

FIGURE 8-17. TEST NO. 2 - ENDURANCE PREDICTION HISTOGRAM

Table 8-4 shows the same type data as Tables 8-2 and 8-3 for the initial lot of NCR2810's. Table 8-5 is a similar listing of the data for the thicker nitride 2810's.

From the data it can be seen that some of the newer parts have thinner nitrides than some of the initial lot. Based on the predictive measurements the general trend, however, is to thicker parts and is reflected in the improved endurance performance. While the trend intra-lot is along the predicted lines (regarding endurance) devices with similar post soft erase V_T's inter-lot show improved endurance for the new lot. A larger data base is needed to resolve this question.

Figure 8-18 and 8-19 show thick and thin endurance characteristics of the initial lot. The thick part (Figure 8-18) will meet the 3 year retention after 10^4 E/W cycles while the thin part degrades significantly at 10^4 E/W cycles.

Figures 8-20 and 8-21 show thick and thin nitride part for the new lot, respectively. From examining the data on all the curves it is apparent that the new parts have increased endurance and that the thicker nitride parts have the best endurance characteristic. Figure 8-20 shows that the new thick parts will meet the 3 year retention requirement after 4 x 10^4 E/W cycles. The thin part from the new lot will not meet that requirement after 10^4 E/W cycles.

TABLE 8-4. ENDURANCE DATA FOR NCR 2810

Device	Reference Voltage	E/W Cycles	0 Bound Erased at -17V	16V Erases to Fail	Threshold Window at 44 seconds	Slope For Written State Threshold in Volts/Decade			Slope For Erased State Threshold in Volts/Decade			Normalized Retention at 1.4 Volts Window	Correlation Coefficient -1=linear
						Ave	Max	Min	Ave	Max	Min		
320 X		10^0	-6.73	125	6.38	0.445	0.467	0.423	0	0	0	4.02×10^{14}	-0.9996
		10^4			6.34	0.668	0.823	0.356	0.006	0.022	0	1.20×10^9	-0.9924
		3×10^4			6.66	0.983	1.05	0.895	0.017	0.025	0	1.43×10^7	-0.9997
		7×10^4			6.38	1.06	1.18	0.957	-0.021	0.022	-0.107	2.11×10^6	-0.9982
		10^5			6.12	1.08	1.27	0.824	0.012	0.026	0	1.76×10^6	-0.9954
323 ○		10^0	-5.81	22	6.84	0.406	0.467	0.356	-0.006	0	-0.022	1.18×10^{15}	-0.9984
		10^4			6.12	0.952	1.16	0.623	0.006	0.022	0	5.22×10^6	-0.9925
		3×10^4			5.9	1.08	1.29	0.735	0.011	0.022	0	9.19×10^5	-0.9938
		7×10^4			5.78	1.14	1.32	0.757	-0.043	0.044	-0.216	2.70×10^5	-0.9931
		10^5			5.74	1.15	1.35	0.868	0.006	0.025	-0.045	3.86×10^5	-0.9966
327 ▽		10^0	-4.72	1	5.24	0.390	0.490	0.312	-0.006	0.022	-0.022	3.48×10^{11}	-0.9962
		10^4			---	1.20	1.36	1.05	-0.415	0	-0.829	6.44×10^3	-0.9799
		3×10^4			1.52	0.378	0.378	0.378	-0.022	-0.022	-0.022	8.76×10^1	-1
		7×10^4			0								
		10^5			0								
321 △		10^0	-5.07	3	6.3	0.401	0.467	0.334	0	0.022	-0.022	9.61×10^{13}	-0.9967
		10^4			4.98	1.10	1.29	0.824	0.083	0.200	0	1.96×10^5	-0.9906
		3×10^4			---	1.16	1.25	1.07	-0.023	0.065	-0.111	2.23×10^4	-0.9962
		7×10^4			2.3	0.889	1.25	0.526	-0.227	-0.118	-0.337	3.38×10^2	-0.9913
		10^5			---	2.08	3.41	1.36	-1.42	-0.722	-2.05	3.22×10^2	-0.9872
326 □		10^0	-4.71	2	6.27	0.445	0.534	0.401	0.003	0.011	0	6.15×10^{12}	-0.9982
		10^4			4.96	1.03	1.20	0.801	0.022	0.089	-0.022	1.98×10^5	-0.9943
		3×10^4			4.96	1.08	1.21	0.848	0.023	0.074	-0.022	1.21×10^5	-0.9966
		7×10^4			3.98	0.996	1.10	0.868	-0.257	0.400	-0.783	5.58×10^3	-0.9781
		10^5				1.29	1.29	1.29	-0.834	-0.834	-0.834	2.75×10^3	-1
342 ◇		10^0	-4.35	1	5.46	0.395	0.490	0.334	0	0.022	-0.022	1.26×10^{12}	-0.9954
		10^4			4.34	1.10	1.25	0.780	0.028	0.045	0	3.23×10^4	-0.9957
		3×10^4			3.94	1.09	1.25	0.913	-0.008	0.089	-0.134	1.12×10^4	-0.9947
		7×10^4			1.6	0.668	0.668	0.668	-0.067	-0.067	-0.067	8.24×10^4	-1
		10^5			1.14	0.74	0.074	0.074	-0.32	-0.32	-0.32	1.59×10^4	-1

TABLE 8-5. ENDURANCE DATA FOR NCR 2810
(THICKER NITRIDE PARTS)

Device	Reference Voltage	E/W Cycles	0 Bound Erased at -17V	16V Erases to Fail	Threshold Window at 44 seconds	Slope of 0 Bound Volts/Decade			Slope of 1 Bound Volts/Decade			Normalized Retention at 1.4 Volts Window Closed Inch Second	Correlation Coefficient -1=linear
						Ave	Max	Min	Ave	Max	Min		
353 △		10^0	-5.23	2	6.2	0.297	0.36	0.125	0.006	0.027	0	8.97×10^{17}	-0.9837
		10^4				0.867	0.991	0.708	0.008	0.025	0	9.80×10^{6}	-0.9969
		4×10^4				1.05	1.12	0.923	0.023	0.027	0.018	7.73×10^{5}	-0.9987
		10^5				1.09	1.20	0.912	0.020	0.057	-0.022	2.84×10^{5}	-0.9989
354 ▽		10^0	-6.87	120		0.510	1.00	0.114	-0.008	0	-0.024	1.87×10^{14}	-0.924
		10^4			6.68	0.541	0.688	0.445	-0.006	0.021	-0.045	3.10×10^{11}	-0.9967
		4×10^4			6.18	0.747	0.865	0.556	0.007	0.027	-0.022	1.58×10^{8}	-0.9977
		10^5				0.158	1.04	0.874	0.025	0.076	0	3.59×10^{6}	-0.9997
361 ○		10^0	-5.16	3	6.58	0.352	0.407	0.3177	0.002	0.027	-0.018	2.61×10^{16}	-0.9990
		10^4			5.68	0.769	0.944	0.556	0.004	0.045	-0.051	2.44×10^{7}	-0.9915
		4×10^4			5.24	0.912	1.10	0.601	0.011	0.026	-0.02	1.14×10^{6}	-0.9949
		10^5				1.08	1.18	0.969	0.034	0.075	0	2.77×10^{5}	-0.9995
363 □		10^0	-4.41	1	5.96	0.355	0.423	0.292	0.012	0.027	0	1.43×10^{15}	-0.9989
		10^4			4.66	0.977	1.41	0.579	0.015	0.040	0	2.48×10^{5}	-0.9933
		4×10^4			4.24	0.959	1.11	0.637	0.039	0.054	0.022	7.17×10^{4}	-0.9957
		10^5			---	0.951	1.12	0.778	-0.049	0.024	-0.129	3.36×10^{4}	-0.9990
370 ◇		10^0	-6.9	186	6.92	0.145	0.952	-0.717	-0.005	0	-0.18	1.77×10^{17}	(from last 2 points)
		10^4			6.8	0.502	0.656	0.143	-0.004	0	-0.018	2.69×10^{12}	-0.9750
		4×10^4			6.74	0.790	0.878	0.677	0.000	0.023	-0.022	3.75×10^{8}	-0.9988
		10^5				0.922	1.06	0.757	0.033	0.099	0	2.17×10^{7}	-0.9985
375 X		10^0	-7.1	300		0.243	0.243	0.243	0	0	0	2.05×10^{26}	(from last 2 points)
		10^4			6.56	0.522	0.739	0.078	0.005	0.021	0	3.73×10^{11}	-0.9680
		4×10^4			6.94	0.910	1.11	0.821	0.010	0.023	0	6.23×10^{7}	-0.9981
		10^5			5.5	0.986	1.03	0.963	0.017	0.050	0	6.56×10^{6}	-0.999991

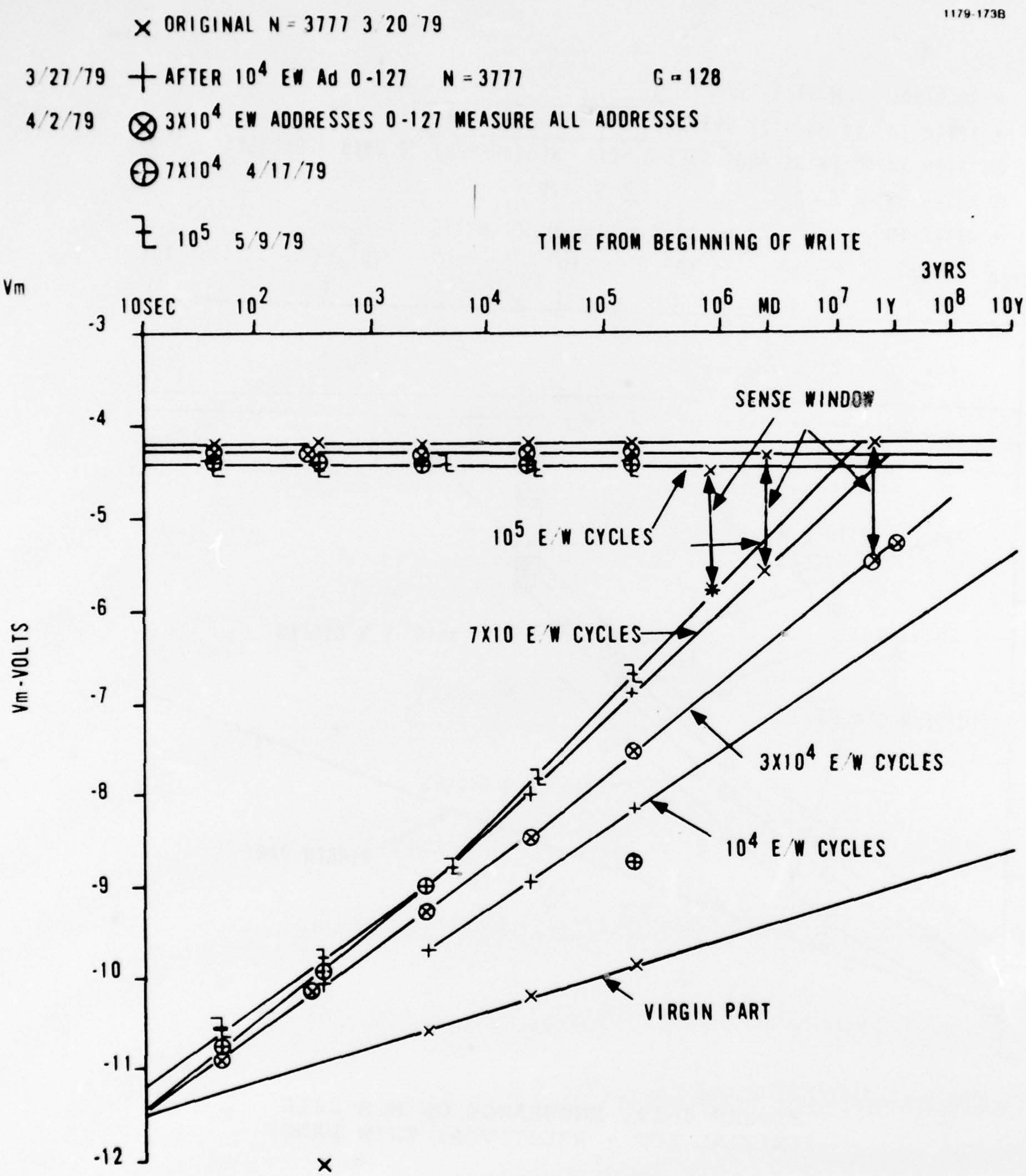

FIGURE 8-18. ENDURANCE OF GI 3400
(RETENTION VS WRITE/ERASE CYCLES)

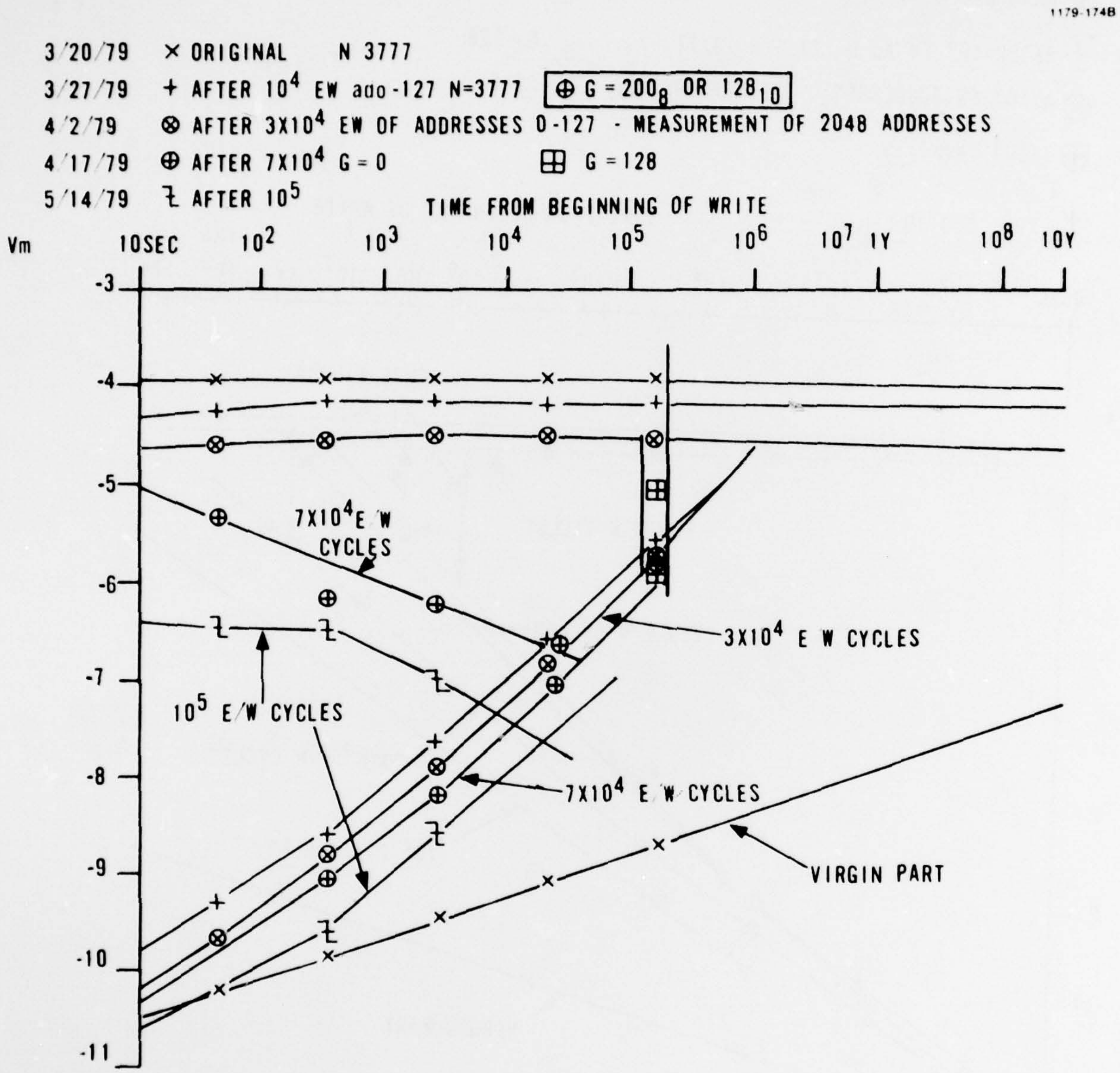

FIGURE 8-19. ENDURANCE OF NCR 2810
(INITIAL LOT - RELATIVELY THIN PART)

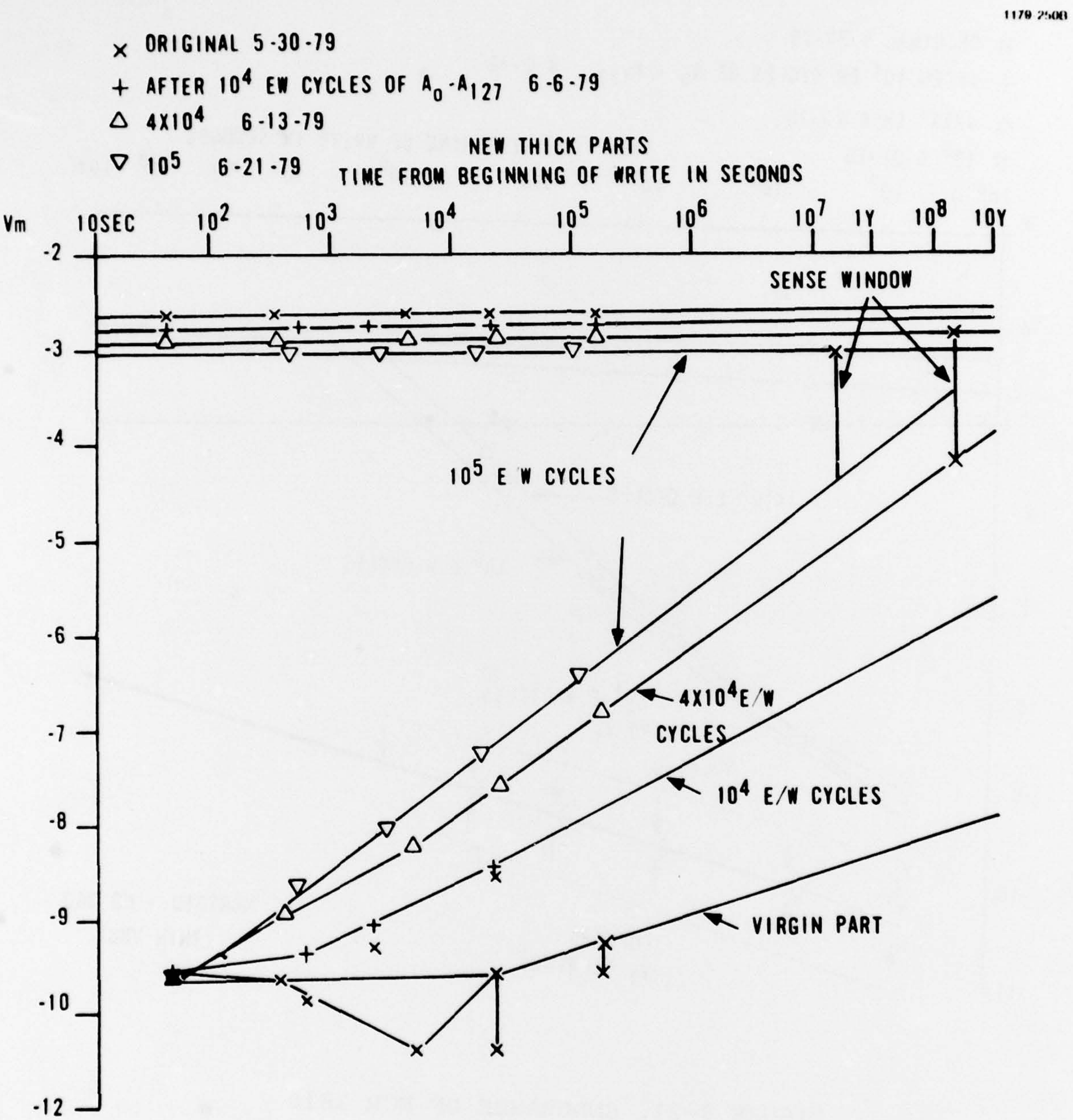

FIGURE 8-20. ENDURANCE OF NCR 2810
(NEW THICK NITRIDE "THICK" PART)

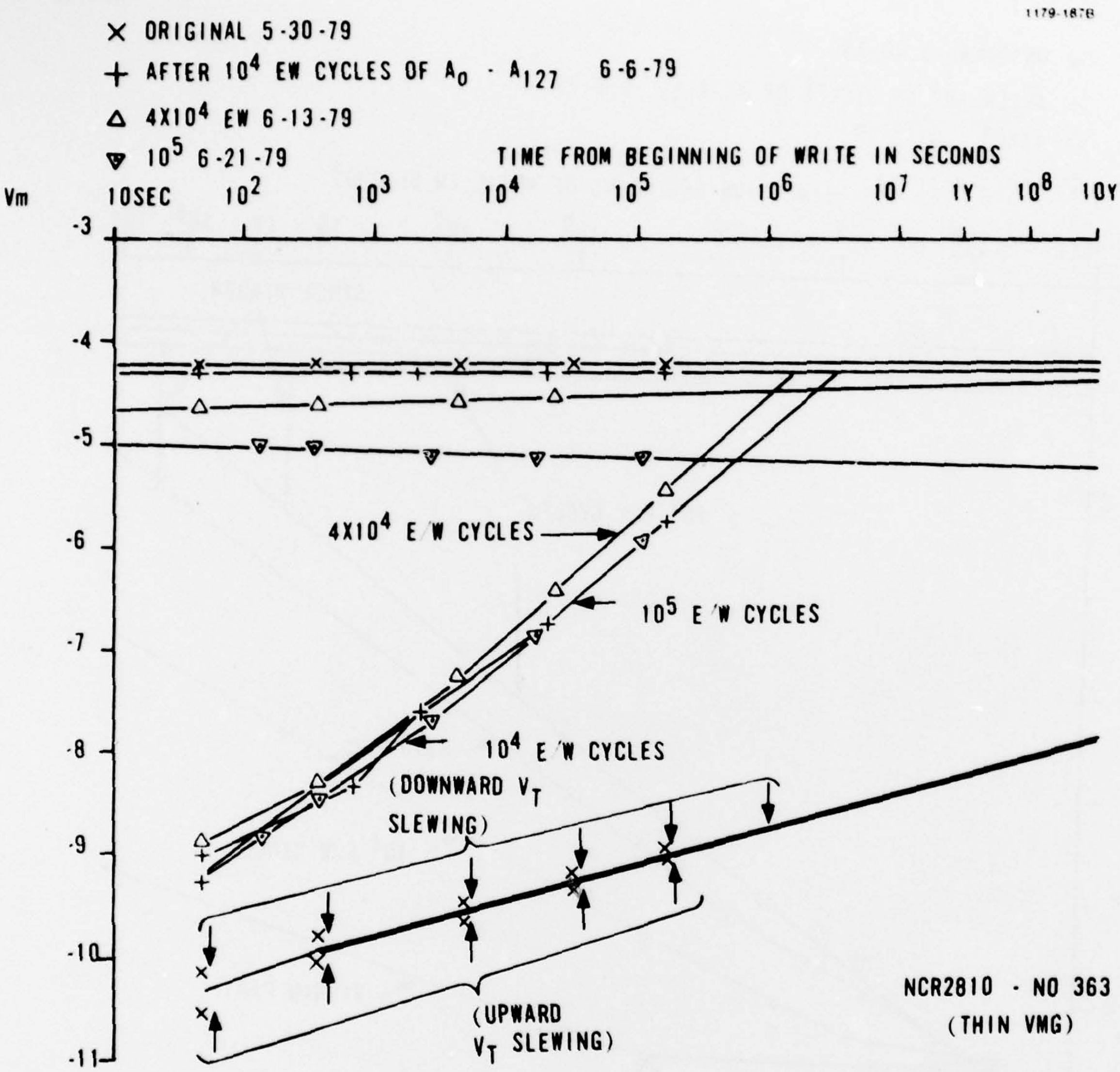

FIGURE 8-21. ENDURANCE OF NCR 2810
(NEW LOT THIN NITRIDE)

Figure 8-26 shows histogram of the predictive data with the endurance plotted on top. The correlation between thick nitrides and higher endurance is further established.

Figures 8-22 and 8-23 show the retention as a function of E/W cycles. The predictive data is labelled on each curve showing the correlation to the endurance of this data. Figure 8-22 shows the endurance of the initial lot while Figure 8-23 shows the new lot data.

8.3.4 GI2401

Figures 8-24 and 8-25 illustrate the endurance of thin and thick nitride parts of the GI2401. The thick part Figure 8-25 meets the MACI three-year retention after 10^5 E/W cycles. The thinner nitride part meets the three-year retention requirement after 3 x 10^4 cycles.

Figure 8-24 shows histograms of the predictive data and plots the retention after 10^4 E/W cycles on top. The general correlation can again be seen between these factors and endurance.

Figure 8-28 shows the retention as a function of E/W cycles for the GI2401. Except for device No. 405 predictive data listed with the plots shows good correlation between endurance and predicted endurance.

8.4 CONCLUSIONS

While no device type showed high endurance the NCR2810 and GI2401 were the best. The predictive measurements showed excellent correlation to the actual endurance with thicker nitride parts clearly superior to thinner nitride parts in this parameter. The predictive data was more accurate for the transistor plus reference row devices (i.e., 2810 and 2401) than the single transistor/cell devices which have internally generated voltage regulation.

No measurements were taken on the 7053 due to the lack of threshold capability limiting the collection of data.

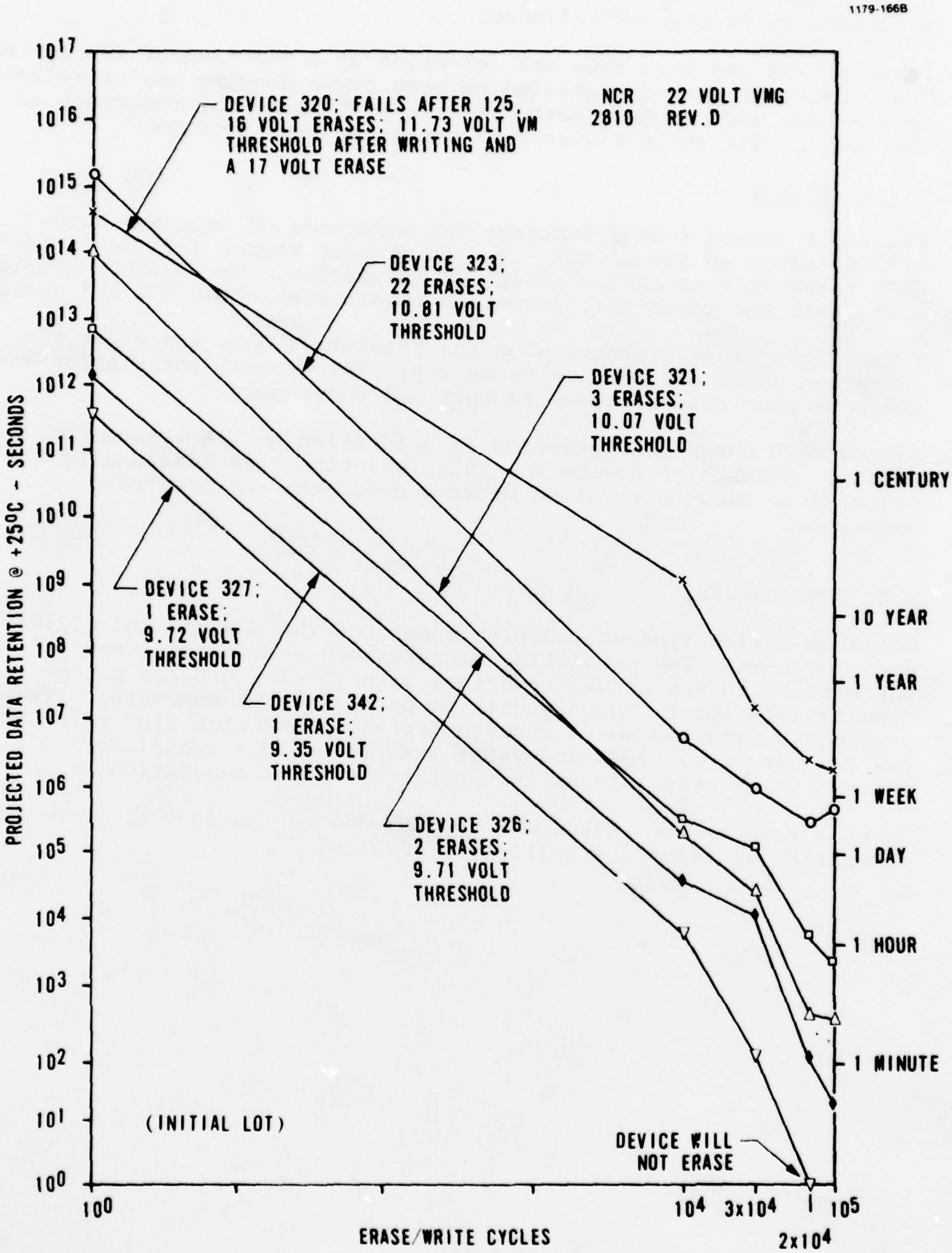

FIGURE 8-22. ENDURANCE OF NCR 2810

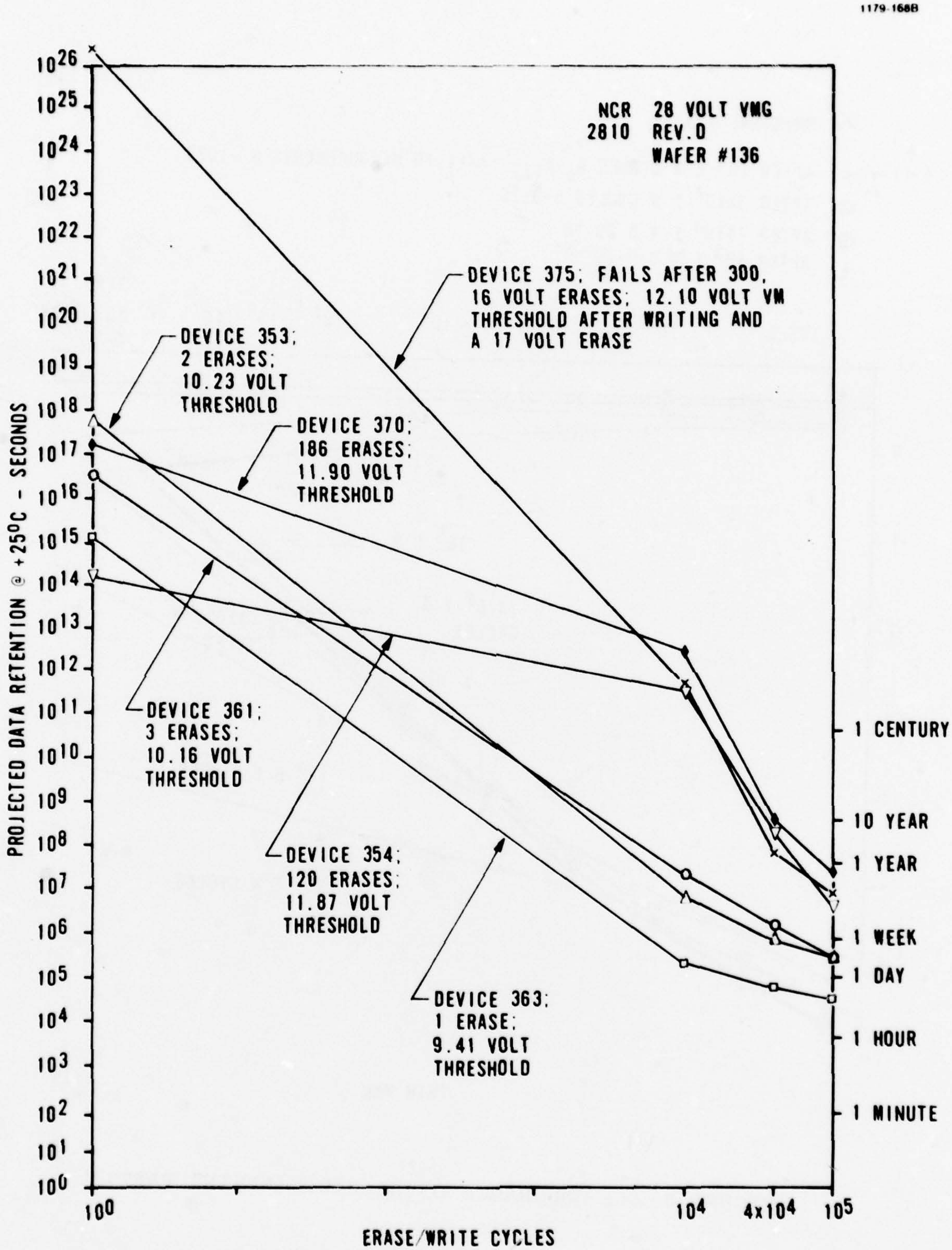

FIGURE 8-23. ENDURANCE OF NCR 2810 (NEW LIST)

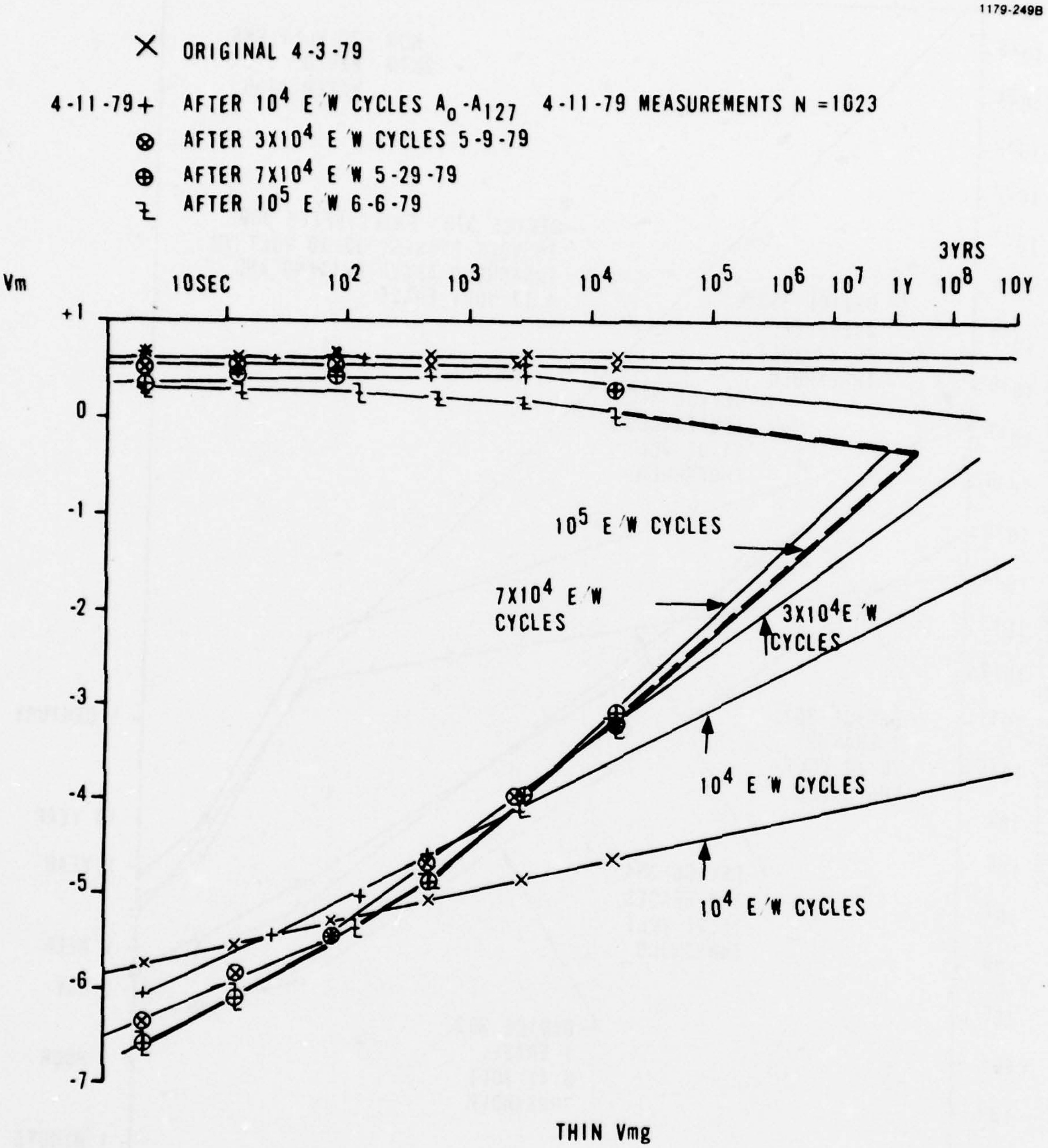

FIGURE 8-24. ENDURANCE OF GI 2401 ("THIN" PART)

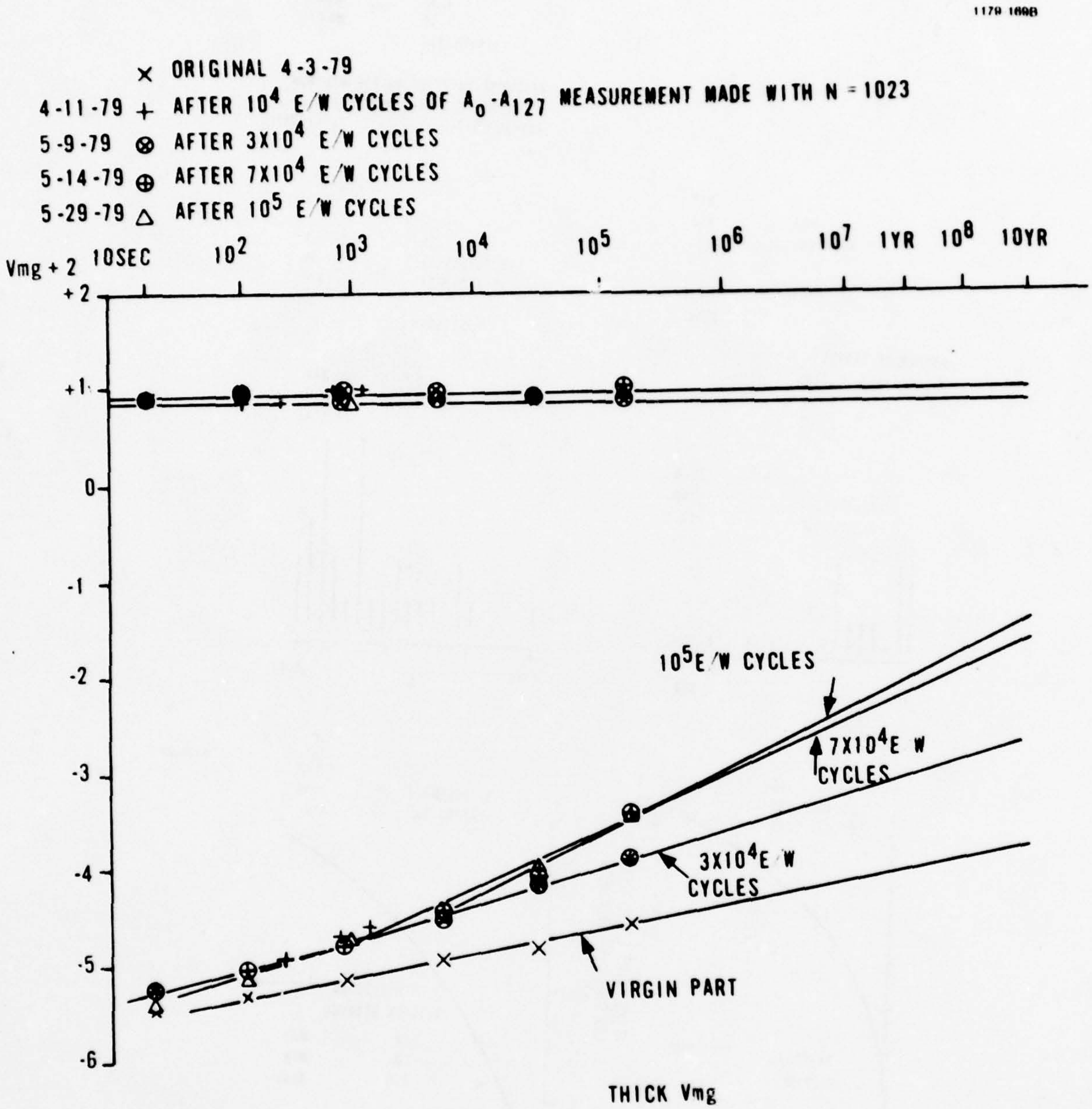

FIGURE 8-25. ENDURANCE OF GI 2401 (THICK PART)

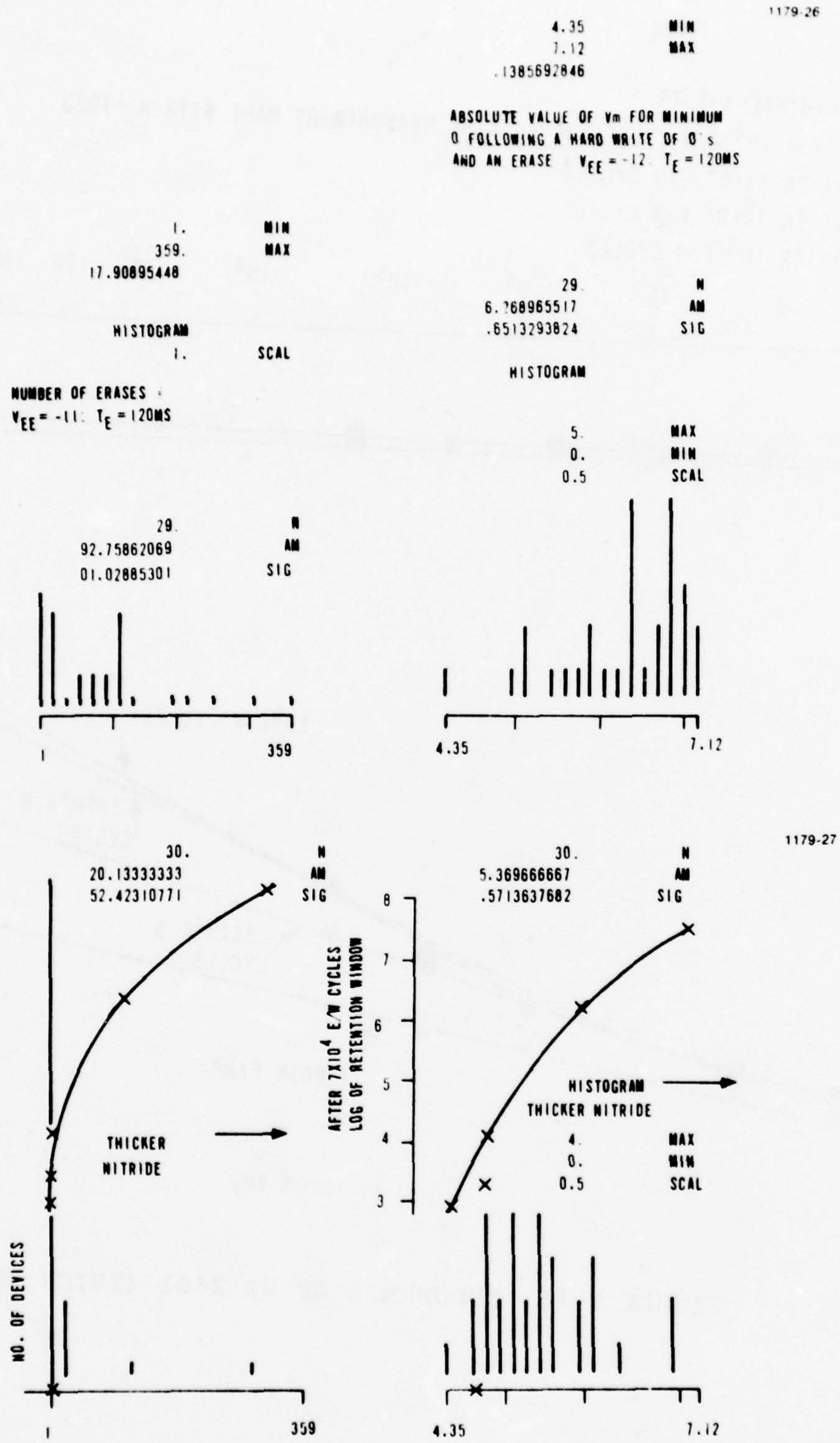

FIGURE 8-26. NCR 2810 PREDICTIVE DATA HISTOGRAM

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5.		2.	
1.		3.8	
390		4.7	
48		3.3	
719		4.5	
39.		3.8	
1.		1.8	
4.		2.	
10.		2.5	
1200.		4.8	
217.		4.2	
73.		3.66	
1.		3.5	
264.		4.7	
1.	MIN	1.8	MIN
1200.	MAX	4.8	MAX
53.9799		.1500750375	
14.		14.	
212.2857143	AM	3.518571429	AM
338.5083727	SIG	1.024373377	SIG

1179-29

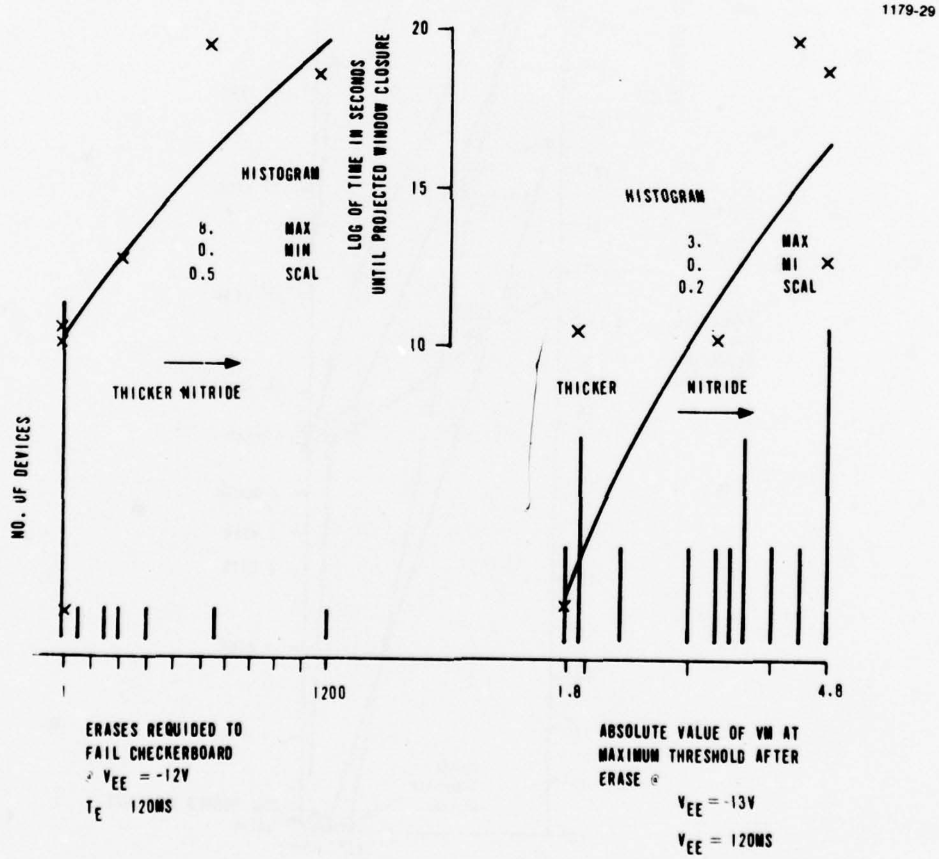

FIGURE 8-27. PREDICTIVE ENDURANCE DATA FOR GI 2401

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2401 ENDURANCE CHARACTERISTIC

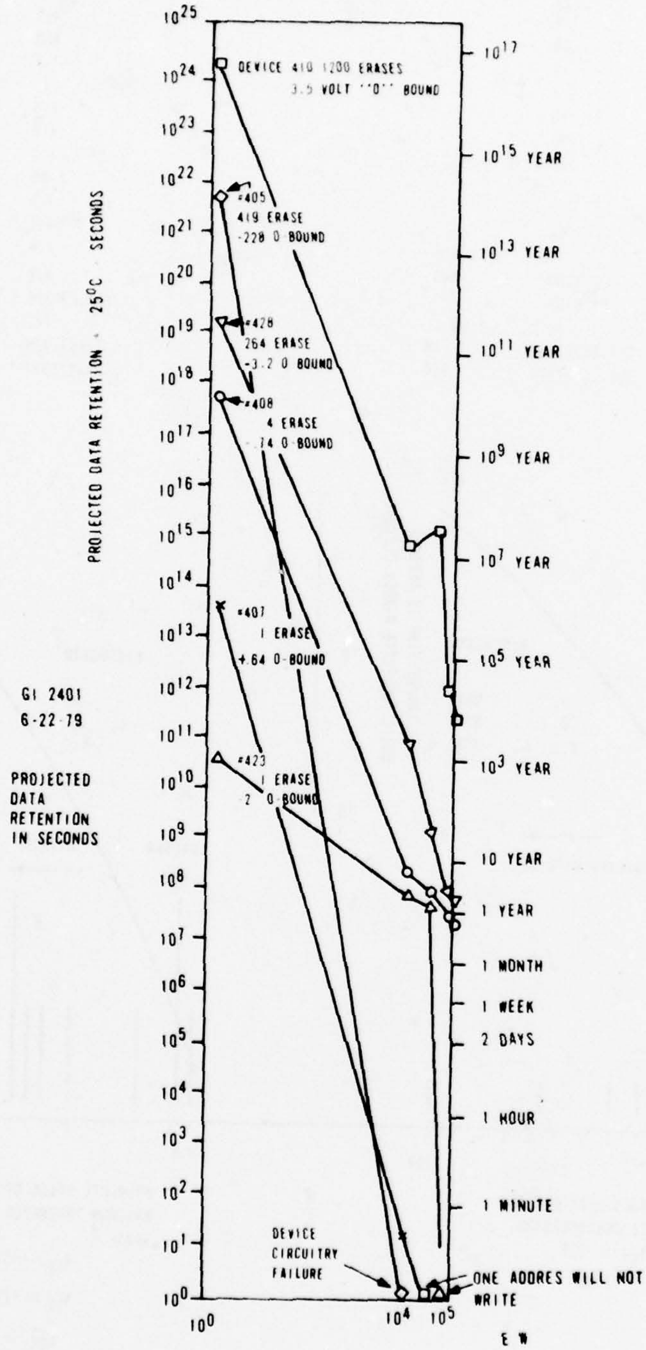

FIGURE 8-28. 2401 ENDURANCE CHARACTERISTIC

Section 9

MECHANICAL AND PACKAGING TESTS

9.1 PACKAGING

9.1.1 Objective

To establish the integrity of various vendor's EAROM packages for use in military applications, or determine what additional processing is necessary to bring the devices up to military standards.

9.1.2 Procedure

The 22 and 24-pin side brazed dual inline packages from National Cash Register (NCR) and General Instrument (GI) and the 24-pin side brazed dual inline packages from Nitron were tested to MIL-STD-883B Method 5005.5, Group D tests, as shown in Table 9-1. Since these devices were electrical rejects, electrical tests have been eliminated. Fifteen mechanical samples of each of the following devices were tested:

Part	Vendor	Package
2401	GI	24-pin
3400	GI	22-pin
2451	NCR	22-pin
2401	NCR	24-pin
7053	Nitron	24-pin

Nitron and NCR use their 24-pin package for the 2810 device, therefore, this device package is the same as the 7053 and the 2401 packages. Details of the tests performed are on file and available upon request.

9.1.3 Results

All devices meet MIL-STD-883B requirements as outlined, with one observation; all packages showed varying degrees of gold tarnishing on the package lids and leads following the Salt Atmosphere test (see Figure 9-1).

9.1.4 Conclusions

Although all packages exhibited tarnishing of the gold surfaces, this should not be cause for rejection. It has been shown from previous studies (Reference 1) that this tarnishing is related to the amount of handling and, therefore, body oils deposited, prior to the salt atmosphere tests. In addition, minute scratches on the gold lid surface aided retention of the oils on the surface. The direct

TABLE 9-1. GROUP D (PACKAGE RELATED TESTS) (FOR ALL CLASSES)

Test	MIL-STD-883 Method	MIL-STD-883 Condition	Sample Size
Subgroup 1			
(a) Physical dimensions	2016		3 devices (0 failures) or 5 devices (1 failure) 5/
Subgroup 2			
Lead integrity	2004	Test condition B2 (lead fatigue)	5 pcs
Seal (a) Fine (b) Gross	1014	As applicable	
Subgroup 3 2/			
Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum	5 pcs
Temperature cycling	1010	Test condition C, 100 cyles minimum	
Moisture resistance 10 day	1004	No electricals	
Seal (a) Fine (b) Gross	1014	As applicable	
Visual examination		Per visual criteria of Method 1004	
Subgroup 4 2/			
Mechanical shock	2002	Test condition B minimum	5 pcs
Vibration variable frequency	2007	Test condition A minimum	
Constant acceleration	2001	Test condition B minimum (see 3), Y_1 orientation only	
Seal (a) Fine (b) Gross	1014	As applicable	
Visual examination	3/		
Subgroup 5			
Salt Atmosphere	1009	Test condition A minimum	5 pcs
Seal (a) Fine (b) Gross	1014	As applicable	
Visual examination		Per visual criteria of Method 1009	

2/ Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "mechanical"

3/ Visual examination shall be in accordance with Method 1010 or 1011.

5/ Test three devices; if one fails, test two additional devices with no failures.

6/ Subgroup 1 devices may be used for subgroup 2.

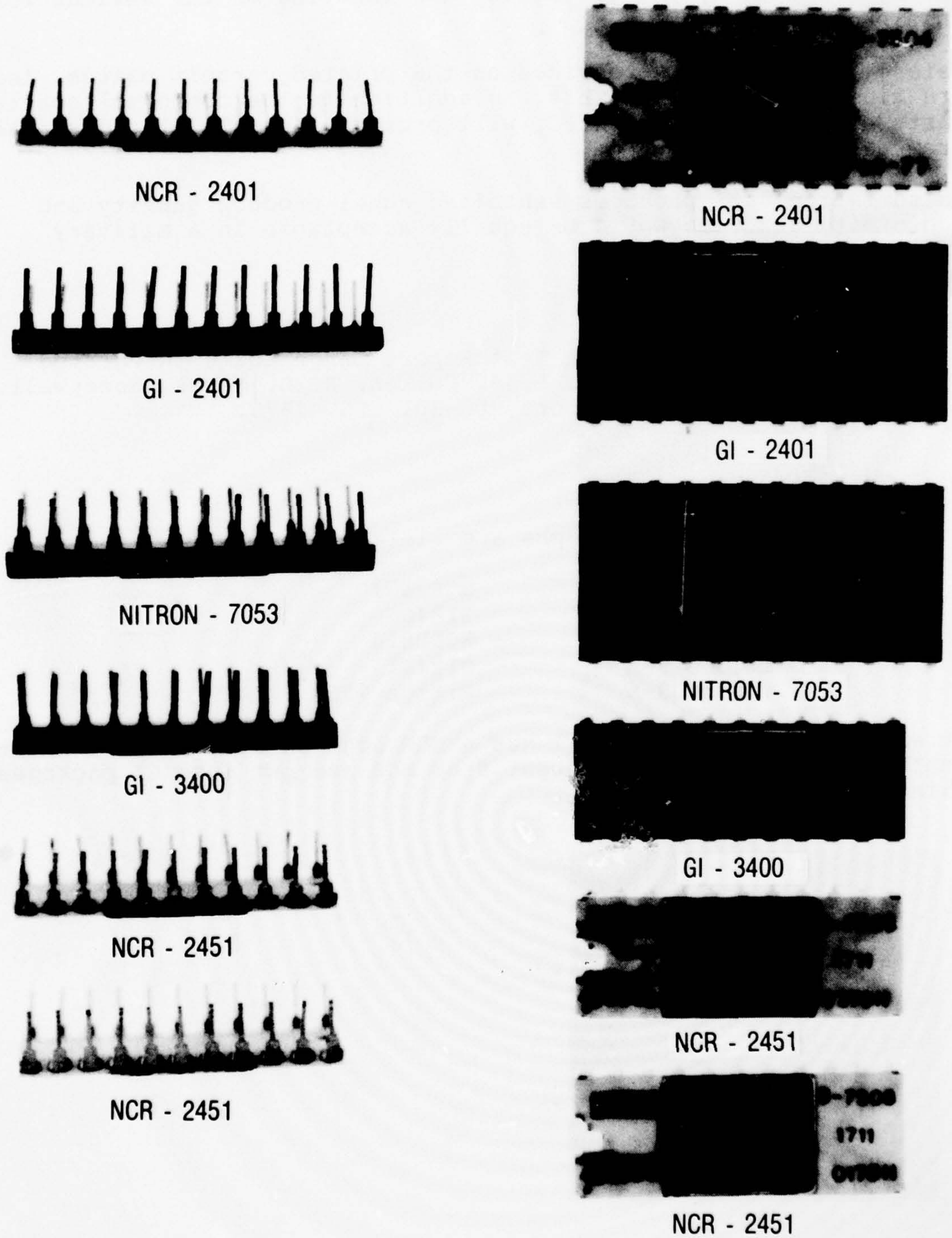

FIGURE 9-1. WORST CASE SALT ATMOSPHERE SAMPLES

contact can be eliminated in normal manufacturing and processing by the use of gloves. However, if the direct handling of devices can not be eliminated, the processing and mounting of the devices solves this problem.

Before mounting of the devices on the printed circuit boards, leads are tin-solder dipped. This, in addition to the conformal coating of parts after they are mounted, will protect the gold plated surfaces from salt tarnishing.

In summation, all packages exhibited equal product quality and conformity and each would be equally acceptable in a military application.

9.1.5 References

(1) "HDC-301 Qualification Test Report Large Scale Integrated Circuits, Addendum A", R. A. Cullen, R. G. Novak, Honeywell Qualification Test Report HDC-301 CPU, 1975.

9.2 CHIP LAYOUTS

The following photomicrographs are listed below:

Figure 9-2	NCR2451
Figure 9-3	GI3400
Figure 9-4	NCR2810
Figure 9-5	GI2401
Figure 9-6	Nitron 7053

It was noted that the GI2401 has a NCR logo on it. It is unknown whether these chips were bought from NCR and put into GI packages at this time.

C7905-124

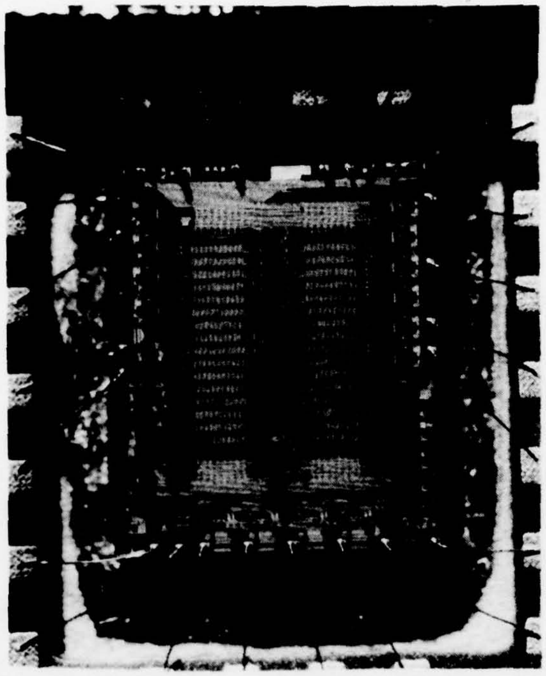

FIGURE 9-2. NCR 2451

C7905-125

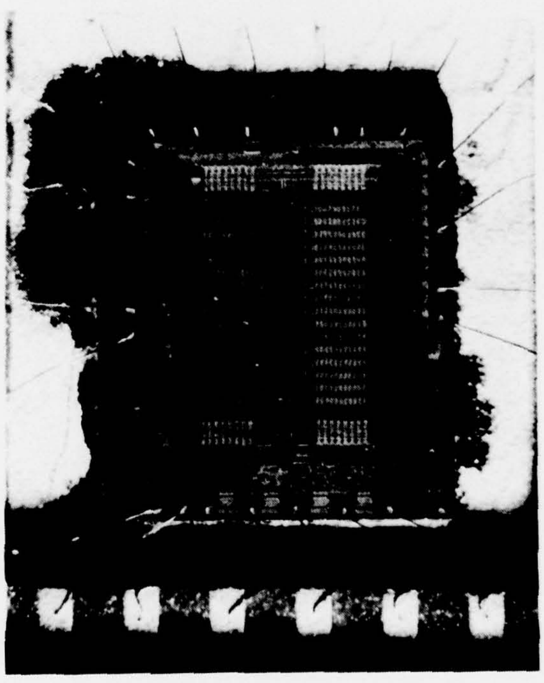

FIGURE 9-3. GI3400

C7905-122

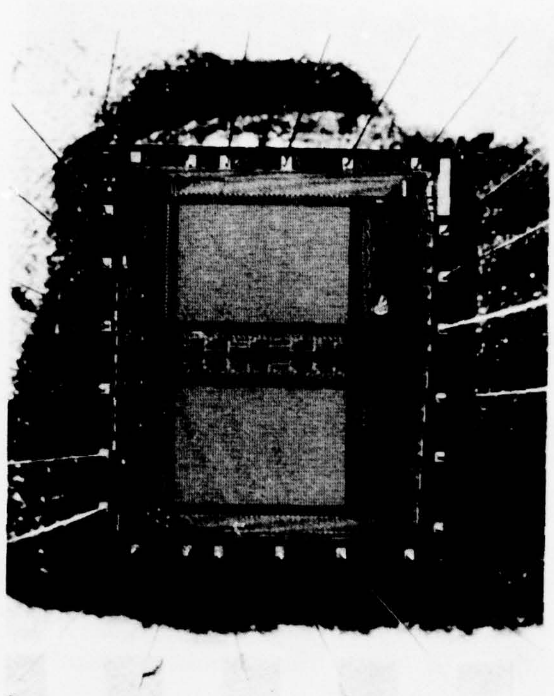

FIGURE 9-4. NCR 2810

C7905-123

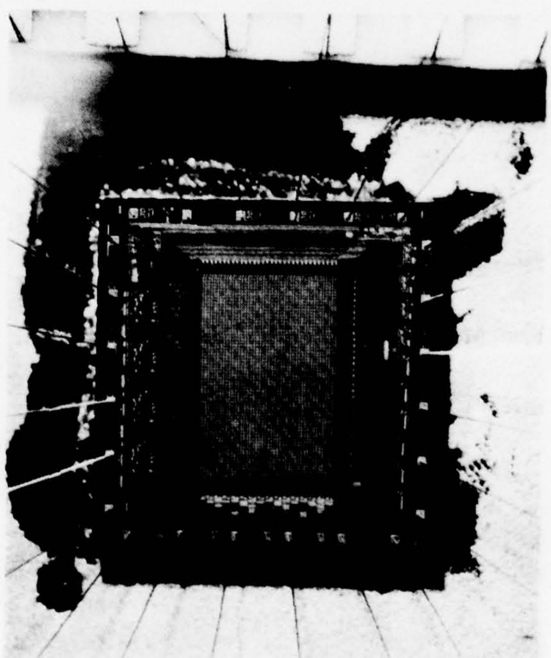

FIGURE 9-5. GI 2401

C7908-156

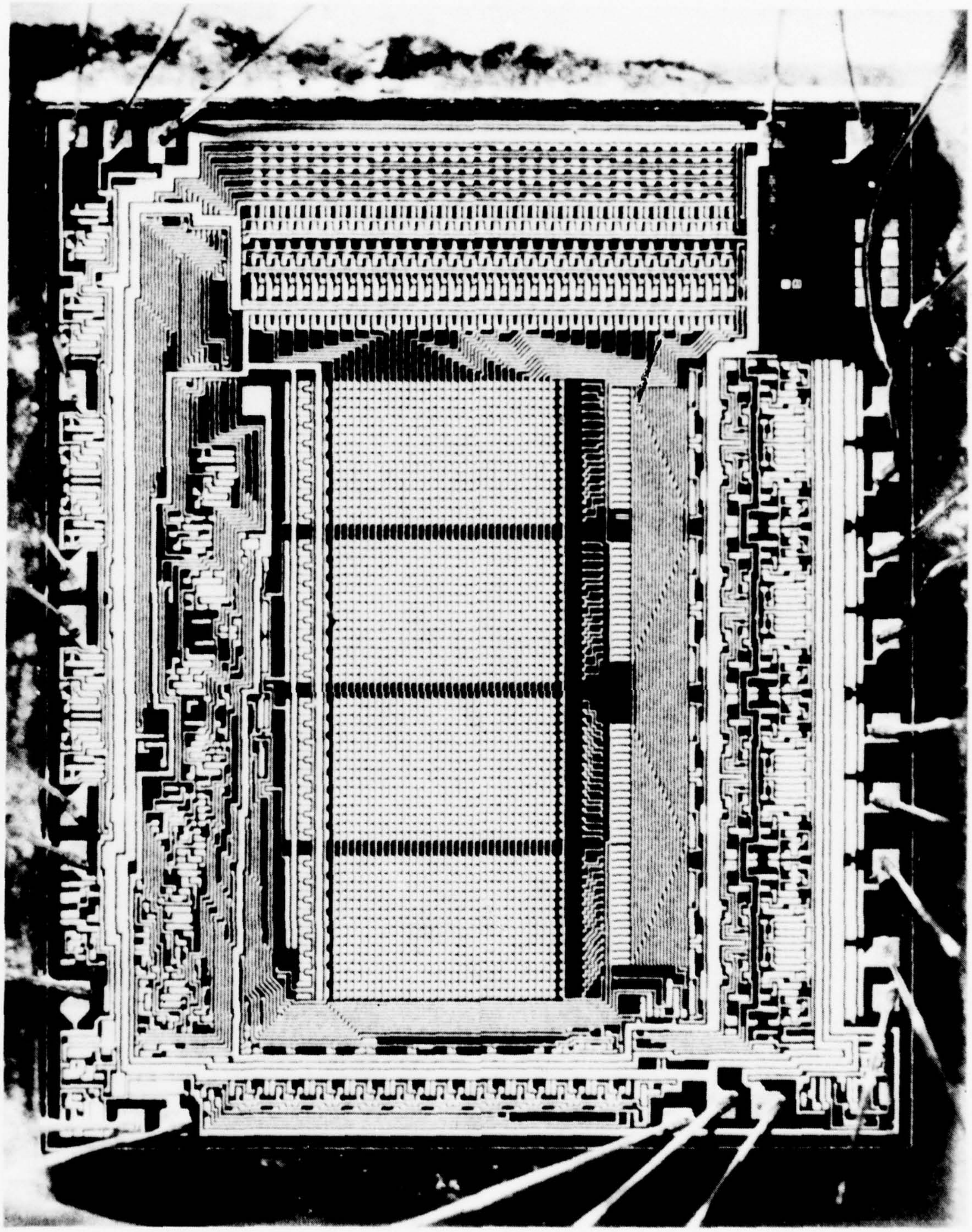

FIGURE 9-6. NITRON 7053

Section 10

CONCLUSIONS

Since some additional data has yet to be assimilated into the comparative study of the candidate MNOS device a comparison matrix would not be complete. The second interim report will include the remaining data (i.e., primarily dc parameters) integrated with the present data with a comparative matrix that will attempt to guide potential military users of MNOS devices to an optimum solution to device selection for their system.

10.1 NCR 2810

10.1.1 Advantages

This device is superior to all others in cost per/bit, number of sources, retention over temperature, radiation resistance, density and performance over temperature. In addition it shares the spotlight as the best endurance, has most support, and low read mode power.

10.1.2 Disadvantages

Disadvantages of this device include the number power supply voltages and switching of power supplies required, marginal access time for some microprocessor applications, EAROM organization, high write power, large package.

10.2 NCR 2451/GI 3400

Since these devices are similar, they are taken together.

10.2.1 Advantages

Some advantages of the NCR 2451/GI 3400 are: best access time, good temperature operation, best organization, no power switching required, low write mode power, smaller 22-pin package, simple threshold measurements, edit capability, faster writing and erasing.

10.2.2 Disadvantages

Some of the disadvantages of these devices are: lower endurance, less dense, higher cost, voltage sequencing sensitive.

10.3 GI 2401

10.3.1 Advantages

Advantages of the GI 2401 are: more mature part high retention and tied for best endurance capability, low read mode power, good radiation resistance, low cost.

10.3.2 Disadvantages

Disadvantages of this device are: no future support, slow access time, low density, power switching required, exhibited intermittant V_T measurement performance.

10.4 NITRON 7053

10.4.1 Advantages

Internal/external clock operation, two-transistor cell potentially good in radiation are advantages of the Nitron 7053.

10.4.2 Disadvantages

Disadvantages of the Nitron 7053 are: low density, poor temperature performance, no threshold measurement capability, high cost, single source, questionable future support, slow access time.

The tentative selection of second-phase devices is both the 2451/3400 and the 2810. Preliminary approval has been given by ERADCOM.

ATTACHMENT A

1178-15565 15 November 1978

Contract No. DAAB07-78-C-2935

MNOS DEVICE FOR MILITARY
AND AEROSPACE APPLICATIONS

TASK I REPORT

Prepared by

R.L. Wiker

Honeywell

AVIONICS DIVISION
ST PETERSBURG FLORIDA

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Section 1

INTRODUCTION

Many military and aerospace data processing applications require the use of nonvolatile and perhaps even nondestructive readout (NDRO) memory devices. For years, and to some extent even now, magnetic drums and their small magnetic disk derivatives were the only solution to the problem. These serial readout devices limited processing throughout and were followed by memories implemented with other magnetic technologies. Examples of these are thin films, biaxial cores, toroidal cores, and plated wire to name the more important ones. Magnetic bubble memories have entered this scene in only the last few years.

Each of these magnetic memories has provided a solution to the various design problems with which the military data processor designer has had at the time. Each has filled a particular functional niche. Yet, each has had limitations, some of which are:

- High cost
- Risky technology
- Bulky form factors
- High power dissipation
- Awkward electromechanical configurations
- Temperature problems
- Low repairability
- Moderate but insufficient speed
- Requirements for multi-voltage
- Low to moderate storage density

With the emergence of the semiconductor memory technology, many of the problems mentioned above can potentially be overcome. These devices can offer low cost memories and can be packaged on planar modules (circuit boards) which fit a wide range of applications, their power dissipation can be low (and power switched) and they have been operated successfully over wide temperature ranges in a multitude of vigorous environments. Further, because of their circuit chip implementation troubleshooting can be accommodated easily and repair effected in a most economical fashion. Storage density (bits per square or cubic inch) are always on the rise, as is the performance at the circuit chip levels. 16,000 (16K) to 64,000 (64K) bit chips (one circuit) are here now, with further expansion in sight. Read access times are in the low nanosecond region, easily surpassing core and plated wire memories - the current two big names in military configurations.

The number of chip organizations, performance levels, and technology types available in semiconductor memories is enormous. There are read only memories (ROMs), programmable read only memories (PROMs), random access memories (RAMs) and others implemented in bi-polar, N-channel MOS, P-channel MOS, current mode logic (CML, ECL, etc.), and an infinite variety of technologies. The trend is to provide the most dense

memory devices possible with the highest speed performance with the lowest accompanying power dissipation at the lowest cost. Even with these forward strides there are still applicational problems with semiconductor memories.

Semiconductor ROMs and PROMs suffer from their unchanging nature. Once they are programmed the data stored cannot be changed. In other words they are truly nonvolatile and NDRO. These fast memories serve admirably as program stores where once programmed there is no need for changes.

On the other hand, semiconductor RAMs are fast but the devices are volatile. If power is lost in the system, all programs, data or calculated results are immediately lost. They can serve then only as scratchpad memory or in memory organizations where loss of stored data can be accommodated in other ways or the loss is not critical to the system functionality.

A combination of the semiconductor ROMs and RAMs in a memory configuration has proven to be a very effective organization. The nonvolatile ROMs can be used for the program memory and the RAMs for scratchpad. Yet, the nonchanging character of the ROM is still a possible problem. For the mature system where there is no need to change the program the solution is satisfactory. For many system applications the permanent nature of the storage cannot be tolerated.

A recently developed technology overcomes the limited use of ROMs in some applications. Metal Nitride Oxide Semiconductor (MNOS) devices organized as Electrically Alterable Read Only Memory (EAROMs) chips, Word Alterable Read Only Memory (WAROMs) chips and Block Oriented Random Access Memory (BORAMs) chips have become available. These devices can serve as building blocks to synthesize small to large programmable (by the processing portion of the data processor) memories which are nonvolatile and NDRO. Only the first two device types will be considered further in this paper. The first two afford parallel readout capability and are, therefore, useful over a wide application range. The EAROM and WAROM devices can be procured from a number of sources in the commercial market place. The BORAM, on the other hand, is a serial read out element and while potentially useful in some memory organizations has limited use in military applications because of the sole source nature of its availability.

The purpose of this paper is to demonstrate the applicability of MNOS EAROMs and WAROMs to a number of military and aerospace applications. In particular, the flexibility of memory modules will be demonstrated where "standard" modules can be evolved which can be used in space configurations, in standard aircraft rack configurations and in the Navy's SEM, SAM and ISEM configurations. Further, a series of applications will be postulated ranging from small parallel memories for microprocessor based systems to large serially organized memories which are potential substitutes for disk-type storage systems.

The paper first describes those characteristics of MNOS that make it useful as a military nonvolatile memory. Shortcomings of the devices will be discussed. Next the use of MNOS devices as program memories will be described followed by a discussion of its use as a serial readout mass memory. Finally, a discussion will be provided of concepts in the development of memory modules using MNOS which can be extended into the applications discussed.

Section 2

APPLICATION OF MNOS DEVICES

To Optimally apply MNOS EAROMs and WAROMs, the pecularities derived from the foregoing discussions must be understood and dealt with. The characteristics of principal interest include the:

a. Electrical write capability.

b. Relatively slow write time required.

c. Data retention and its relationship to the write process.

d. Block oriented erase of the EAROM.

e. Word oriented erase of the WAROM.

f. Moderately fast read time.

The electrical write capability (or storage modification within the processing system) eliminates the principal problem with the conventional ROM or PROM and the unique EPROM (a form of storage device modifiable by ultraviolet (UV) light directed upon the chips themselves through appropriate "windows"). The electrical alterability of the EAROM/WAROM accommodates real time and near-real time data processing in many military systems. While the processing throughput is not as great as with ROMs because of the slower read speeds of the EAROM/WAROM, the ability to modify portions of or all of the memory by electrical means can be a decided advantage.

Because of the unique characteristics of MNOS some of the more apparent applications include:

- Parallel readout program memory where the contents of the store may be changed by either processor action or by auxiliary test or support equipment.
- Special data store for constants, or equivalent end point data that are changed infrequently and can tolerate the slow write time. Typical of such memory systems are those required to establish missile aim points, aircraft flight parameters, etc. Such an application is the equivalent of a point of sale terminal memory in a commercial application.
- Special store for codes necessary for processing secure information where the codes must be changed on an irregular or random basis.

- Data recording where the relatively slow data rate can be buffered into the store such as in flight recorders or instrumentation (strain gage, etc.) recorders.

- Serial digital data recording as a substitute for mass media such as tape or disk where the data rates can be managed by buffering.

For this paper, two examples of MNOS applications are examined. One is an MNOS application as a program and constants memory for a 16-bit microprocessor. This memory, designed by Honeywell for a missile application, has been used by the Navy in the ATIGS program, the Army in the SIG-D program, and the Air Force in the DINS program. It will be discussed in more detail in Section 4. The second MNOS application is as a mass memory where Honeywell studies have shown the suitability of these devices to large serial oriented storage systems. This application will be discussed in a subsequent section.

MNOS memories are not a panacea. They are not a cure-all for the problems associated with other systems. However, they are capable of filling the voids left that others cannot adequately fill because of problems in cost, size, power density, etc. The development trend in these devices is such that even some of the current disadvantages will become less severe. With time MNOS techniques might surplant many of the current memory devices and techniques.

Section 3

PROGRAM MEMORY CONSIDERATIONS

For the purpose of this paper, a program memory is defined as the program or constant data store which interfaces with a general purpose processor's read and write mechanization. Typically, these memories are parallel read and write and contain up to 64K words (or bytes) of storage where a word might by 8, 16, 24, or 32 bits in length. Such a memory is ideally applied to microprocessor based systems. Because of the relatively slow write times, however, the MNOS memory cannot be used to provide the high-speed read/write capability needed for intermediate results storage or scratchpad memory. This is a RAM memory circuit function. In addition, MNOS cannot be currently used for the microstore of the processor itself in most applications, a function typically reserved for high speed ROMs. The relationship of the memory types required in normal processing is illustrated in Figure 3-1.

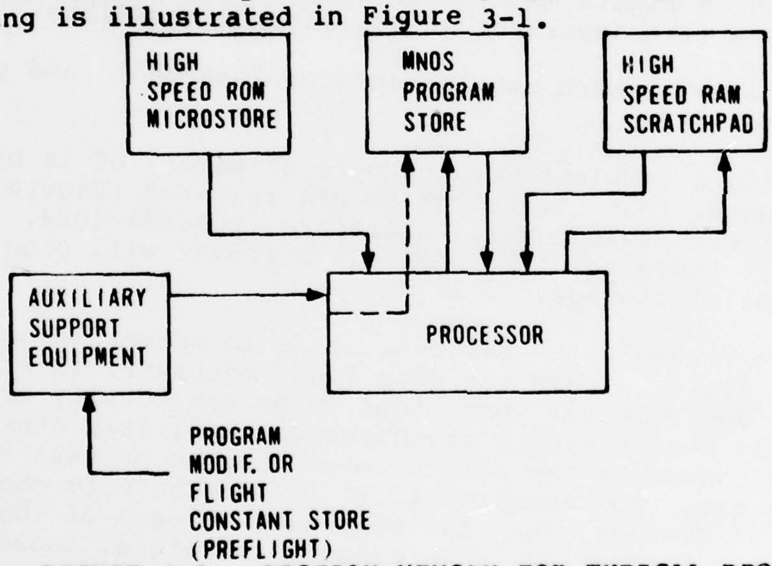

FIGURE 3-1. PROGRAM MEMORY FOR TYPICAL PROCESSOR (MICROPROCESSOR) SYSTEM

Any MNOS program memory functional design includes:

a. Selection of the appropriate MNOS EAROM or WAROM device.

b. Characterization of that device over the expected operational conditions to establish the various voltages and timing conditions at both the chip and memory system level.

c. Determination of the support circuitry necessary to synthesize the complete program memory with the selected MNOS circuit. The chip organization is important in this synthesis.

d. Providing a processor compatible interface for proper control, timing, data transfer, signal buffering and voltage levels.

Other considerations for design of the physical implementation into a module will be considered in a subsequent section.

The MNOS device selected for the design of the ATIGS program memory was the NCR 2401 whose chip organization is illustrated in Figure 3-2. This chip contains 4096 cells or bits broken into four, 1024-cell matrixes, each of which, when addressed, provides a one of 4 bits output. The chip contains row and column decode circuits for addressing as well as sense circuitry and buffering for each of the four matrixes. In addition, there is a chip select circuit for use in addressing at the system level. A subsequent MNOS development was used for the SIG-D and DINS memories in which the NCR 2810 was used. This chip contains twice the bit density as its predecessor and is organized as shown in Figure 3-3. This chip again contains four storage matrixes, a fact important in our later discussions.

With this chip, however, each matrix contains 2048 cells and provides one of four readout.

In order to provide a complete word or byte of memory of 16 bits in length, for instance, four circuit chips are required (Figure 3-4). Four NCR 2401 circuit devices will, therefore, provide 1024, 16-bit words of storage. Likewise, four NCR 2810 circuits will provide 2048, 16-bit words of storage.

In using either of these EAROM devices, it is important to note that, during the erase cycle, a complete chip (four matrixes) is erased simultaneously. For a 16-bit word, four chips are totally erased. Depending upon the memory system organization, auxiliary storage may be required to accommodate the loss of more program or data than was desired during erase. For example, if it is necessary to change only one 16-bit word of storage, then the remainder of each of the bits on the four chips will automatically be erased; therefore, those words must be held in auxiliary storage for subsequent memory reconstruction.

The ATIGS MNOS memory was developed to:

a. Provide 4096 words of program storage.

b. Interface with a bus-oriented 16-bit microprocessor.

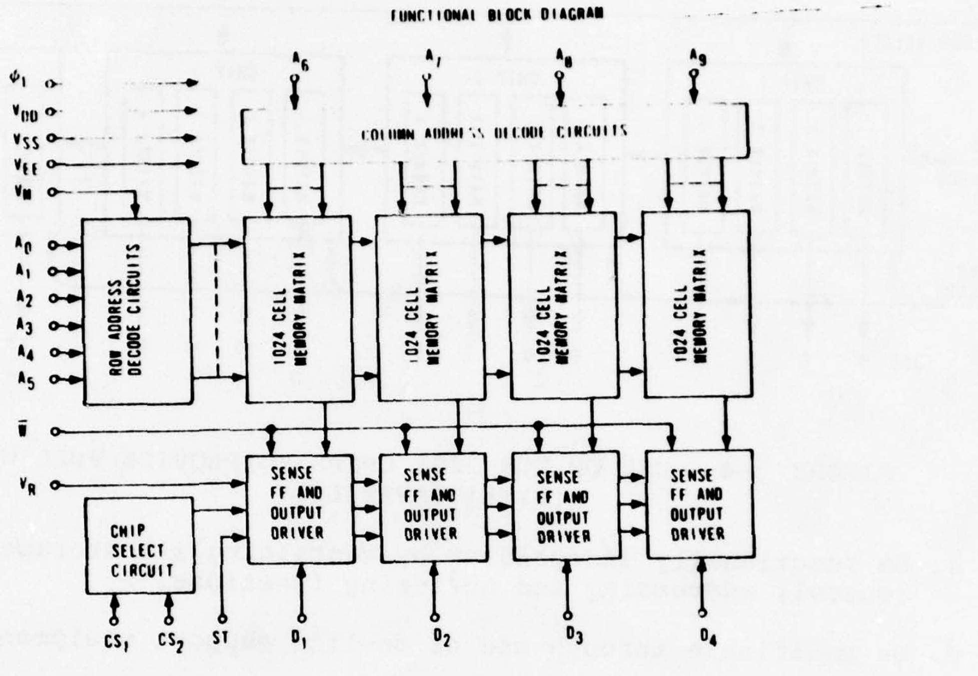

FIGURE 3-2. NCR2401 MNOS CHIP ORGANIZATION

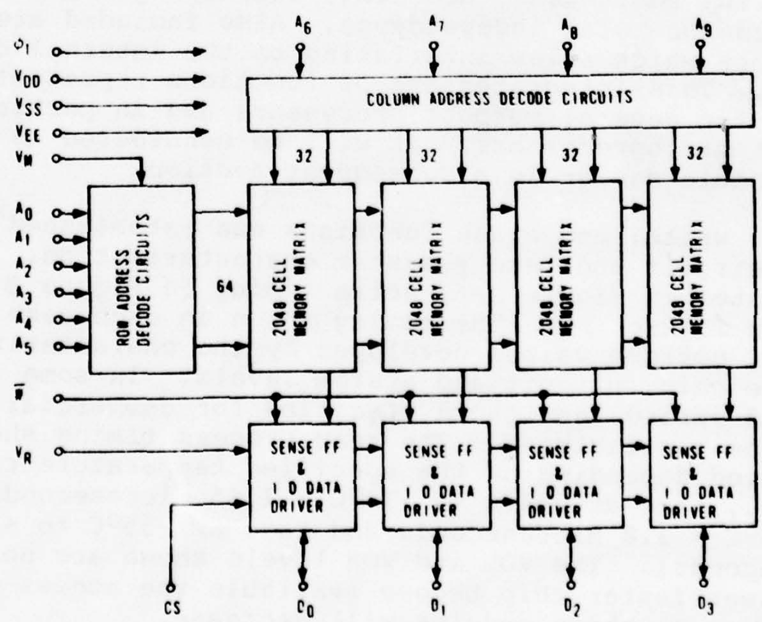

FIGURE 3-3. NCR2810 MNOS CHIP ORGANIZATION

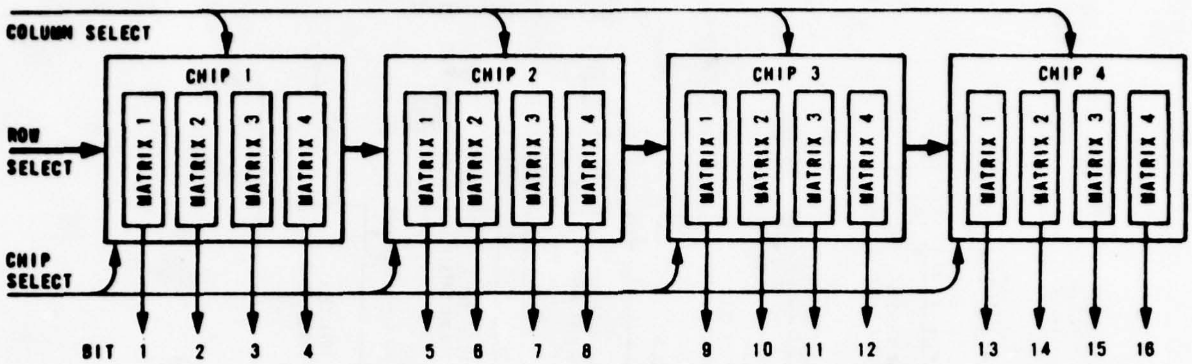

FIGURE 3-4. USE OF NCR 2401 CHIPS TO PROVIDE FULL WORD (BYTE) CAPABILITY

c. Be functionally independent by containing all storage, timing, control, addressing and buffering functions.

d. Be modifiable through use of on-line support equipment.

e. Operate over a wide temperature range in a missile environment.

The organization of the 4096-word memory is illustrated in Figure 3-5. It consists of four arrays of MNOS circuits (four circuits per array) and the addressing, decoding, and timing and control circuitry needed for total independence. Also included are the tri-state buffers which allow interfacing on the internal data processing bus. This integrated set of functions represents an ideal program memory for general purpose processors and in particularly 8-bit or 16-bit microprocessors. It will be considered as a baseline for physical module design in a subsequent section.

Timing of read, write, and erase functions was established through detailed MNOS circuit and memory system characterization. Read timing is illustrated in Figure 3-6, write timing in Figure 3-7, and erase timing in Figure 3-8. The timing shown in each case was selected out of optimum values developed by the characterization programs at the chip, circuit and system levels. In some cases the values selected varied from those specified for commercial range operation by the manufacturer. The read process timing shown in Figure 3-6 varied depending on the specified temperature range of operation (i.e., tacc at -55°C to +75°C = 1.65 microseconds; tacc at -55°C to 95°C = 1.8 microseconds and tacc at -55°C to +125°C = 1.95 microseconds). The VOL and VOH levels shown are normal TTL levels. As newer faster chip become available the access and write/erase times on these modules will decrease.

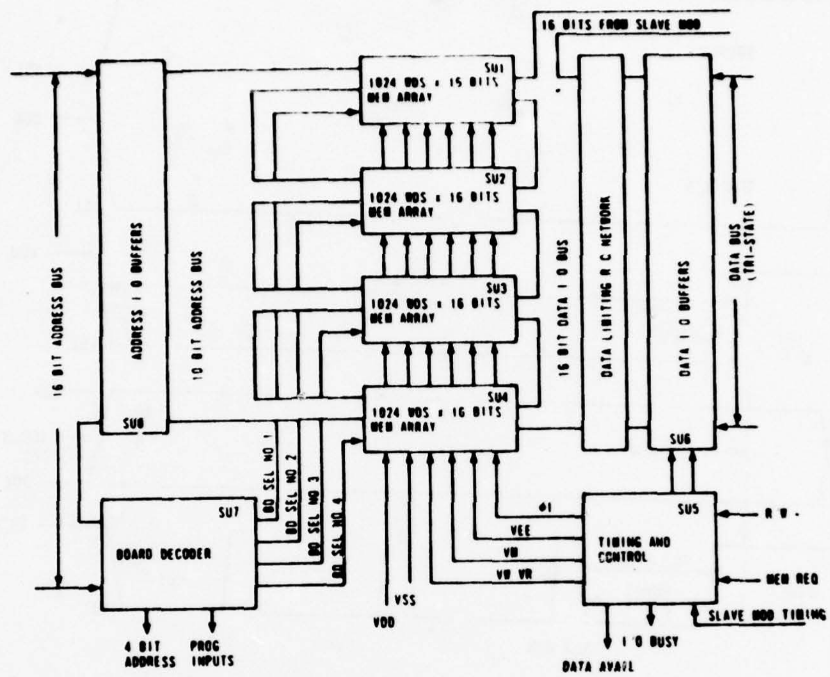

FIGURE 3-5. 4K WORDS X 16 BIT PROGRAM MEMORY ORGANIZATION

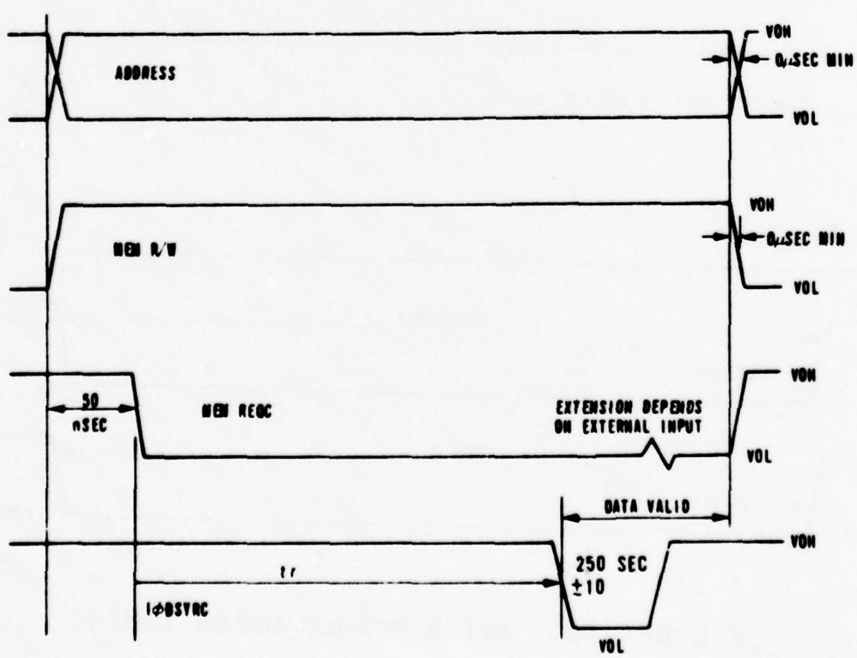

FIGURE 3-6. ATIGS MODULE READ TIMING

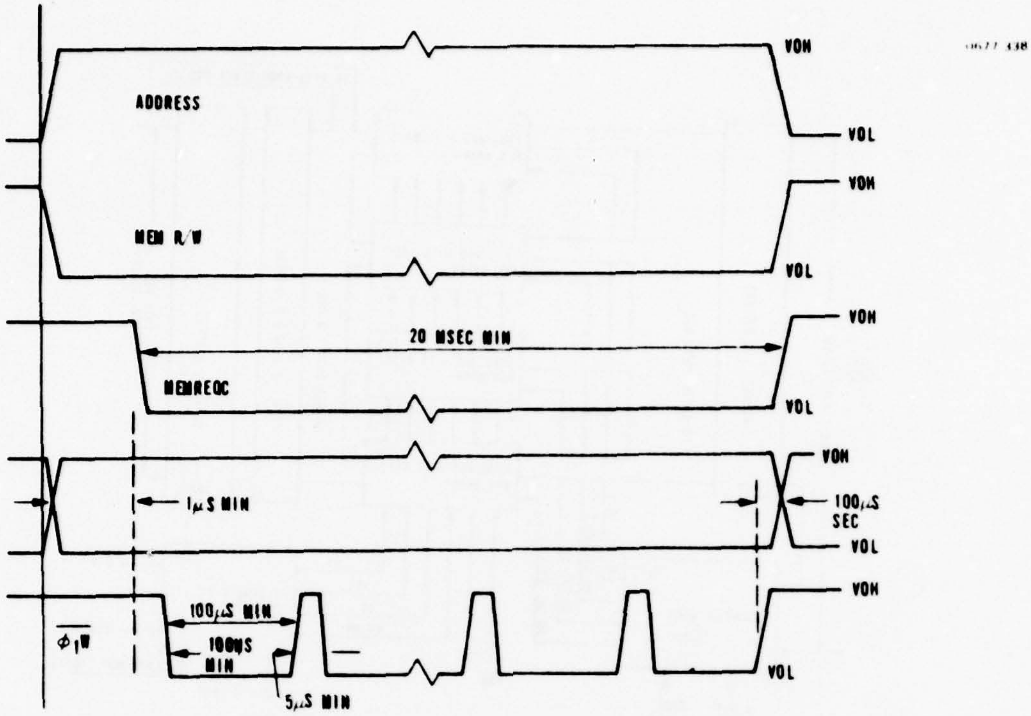

FIGURE 3-7. ATIGS MODULE WRITE TIMING

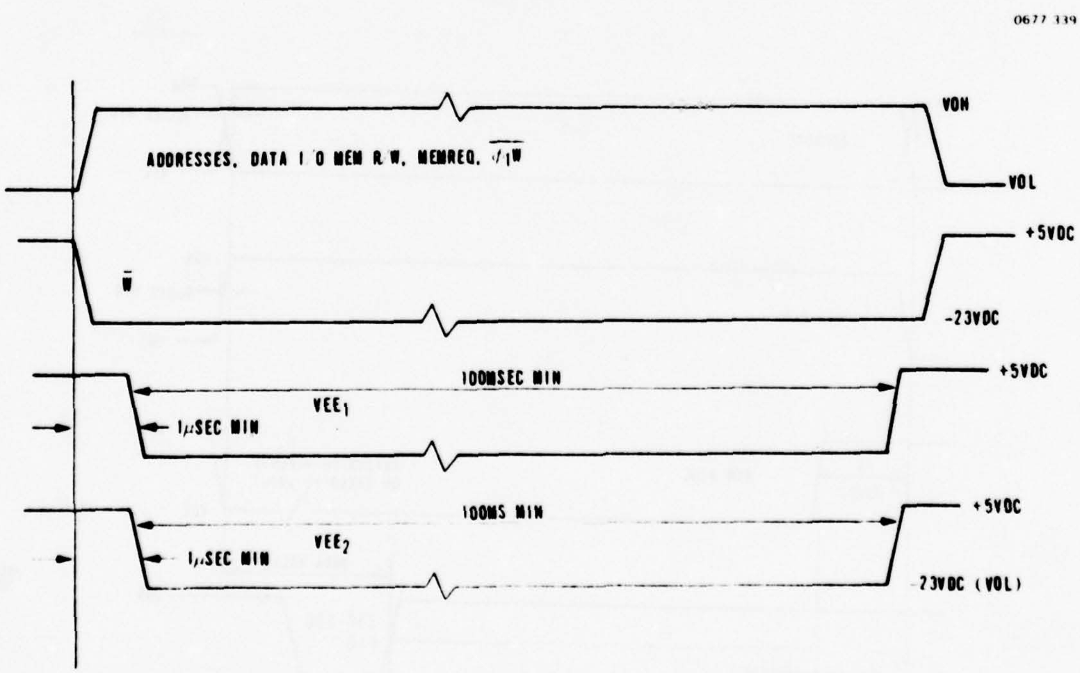

FIGURE 3-8. ATIGS MODULE ERASE TIMING

This functional module is a versatile one which can be applied in several military systems. While writing takes as much as 10 milliseconds, reading of consecutive 16-bit words occurs in one to one and one-half microseconds. Although this is not exceedingly fast, it is more than adequate for many applications.

One of the potential problems associated with the ATIGS MNOS program memory was alluded to in an earlier section. The read speed is such that total processing performance is marginal. This cannot be allowed in some systems and a solution must be found at the systems level. For SIG-D and DINS memories not only is the more dense MNOS circuit (NCR 2810) used but an auxiliary RAM memory is used to solve the performance problem. This high-speed RAM completely maps the data and program stored in EAROM. By duplicate storage of information in the two memories, the nonvolatile, NDRO characteristics of MNOS can be exploited for system reliability and tne high speed of the RAM can be used to improve the performance of the processing system. At the proper time, program switchover from EAROM can be effectively made allowing read speed improvement of better than four-to-one. The functional organization of this memory is illustrated in Figure 3-9.

From the diagram of Figure 3-9, the commonalities with the configuration utilized as in the earlier memory of Figure 3-9,can be seen. This implies that the 4096-word module with self-contained timing, control and buffering can still be used as a baseline physical configuration as discussed later.

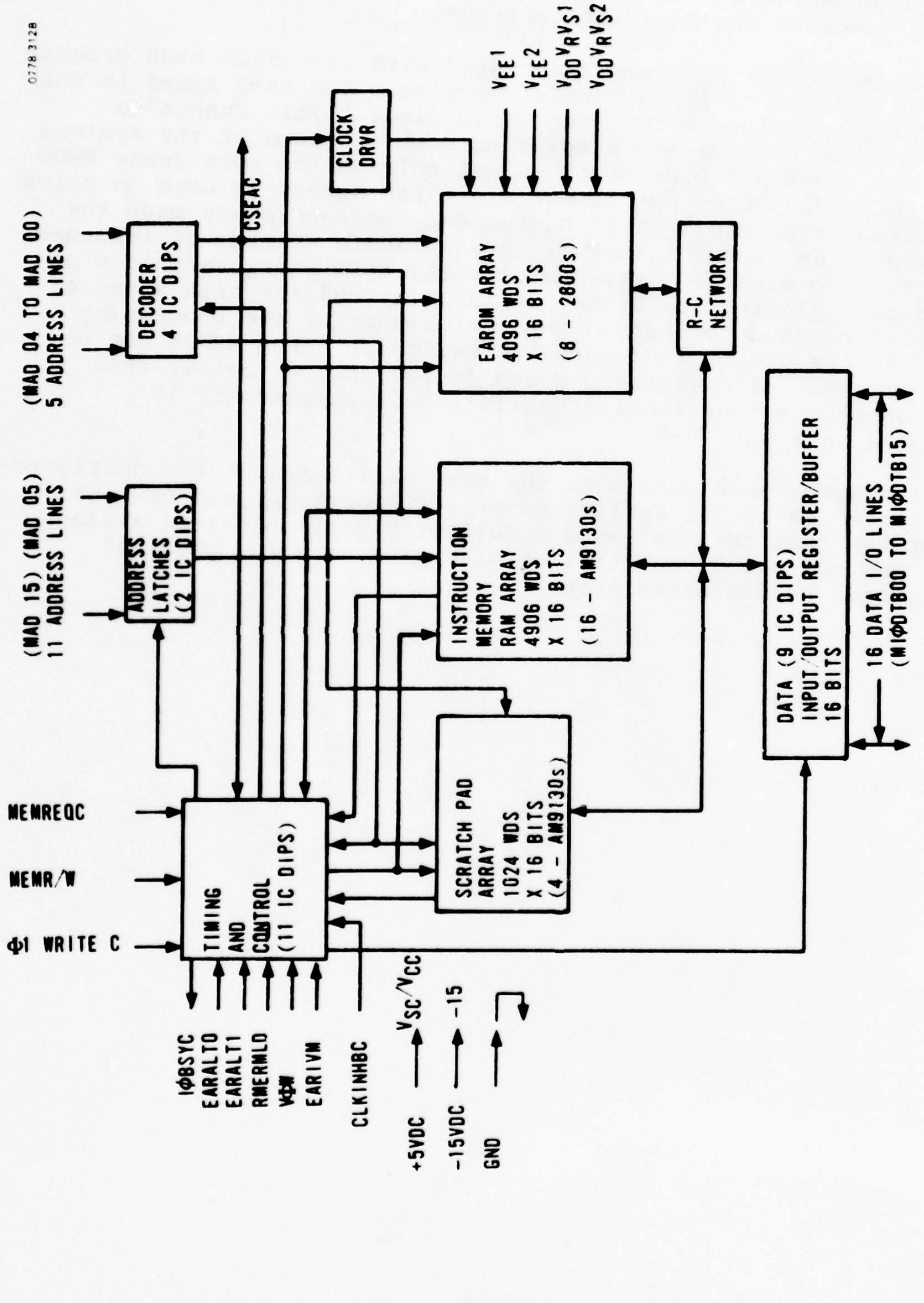

FIGURE 3-9. SIG-D MEMORY

Section 4

BULK MEMORY APPLICATIONS OF MNOS

While MNOS memory does not attain the bit density and low cost per bit of some of the present and proposed military memory technologies, it offers attractive features and expanded environmental and reliability capabilities. Older memory technologies (i.e., drum, tape and disk) attain similar or slightly greater density capabilities, and newer technologies like E-beam, magnetic bubble, and holographic offer potentially greater densities. MNOS presently remains more reliable and usable in military environments.

The inherent reliability and weight penalties that must be paid by drum, tape, and disk systems has made these technologies unattractive for new military designs. Magnetic drums require large rotating masses and employ write and sensing heads that are unreliable, wear rapidly, and require field maintenance. Disk memories (i.e., floppies and fixed head), while not requiring large masses to be rotated suffer from lack of adequate ways of reliably supporting the disk and maintaining head clearance. They also suffer from the same read/write head reliability and maintenance problems in military environments. Tape machines suffer from all of the above maladies with the addition of magnetic tape environmental headaches that are very restrictive. All of the rotating memories suffer from access time latency problems of trying to reach the desired data locations before data can be read or written. Latency places severe throughput limitations on the use in real time situations.

E-Beam, holographic, and magnetic bubble memories resolve the application problems mentioned above to varying degrees if projected capabilities are considered real. All of these technologies are in a relatively low maturity status at present; however. Materials problems and lack of supporting architecture development are limiting applications in military systems.

MNOS devices, while achieving moderate density capability, solve the preponderance of previous memory technology problems related to bulk memory military applications with a relatively mature, well understood technology suitable to dense microcircuit packaging techniques. They offer significant reliability, weight, and power advantages as well as design flexibility over the rotating memories. They offer the environmental and design maturity of the other devices.

The most significant liability of the use of MNOS devices in bulk memory applications lies in the relatively slow write/erase characteristic of the technology. While faster writing MNOS devices are under development, their lack of availability and relatively short data retention characteristic makes their use in new designs risky at this time. This liability can largely be overcome by proper design of the memory organization hierarchy to queue incoming serial data for parallel writing into the memory array thus multiplying the writing rate by the length of the queue. By further mapping of the incoming data with individual bits of the incoming data stream going to separate MNOS chips, an increased multiplication of the writing/erasing rate can be accomplished.

The BORAM structure mentioned earlier is an attempt at the chip level to solve this problem. Figure 4-1 shows the organization of a BORAM chip. While this organization improves the write bit rate from 500 Hz to 32 kHz it limits the flexibilty of outputting data by using "block" access. A read data latency time of a maximum of 33 microseconds is inherent in this approach which may limit throughput in some real time applications.

If standard EAROM or WAROM structures are used in bulk memory applications, this limitation can be overcome by the use of input queuing registers as shown in Figure 4-2. This figure illustrates a bulk memory row page module with a 20-bit input shift register used to queue the incoming data. In the system diagram shown in Figure 4-2, 20-bit data words are shifted into the system input register and dumped in parallel into the page queues. Thus, an input word is broken into 20 parts, one in each EAROM in a similar column. This multiplies the write rate by the number of bits in the page queue times the system queue. The system shown will multiply the write rate by 400. While the system shown has 20 bits in the page queue, a page organized by 32 bits would allow the use of two standard Honeywell Hybrid packages per page. The system shown in Figure 4-4 uses 10 MNOS ISEM modules per page (320K-bit each). Using 20 pages as shown in Figure 4-3, the total system capacity would be 64 megabits (i.e., 3.2K words of 20 bits).

Using a row/column matrix control from the memory controller individual modules in a row page could be selected, while the remainder of modules in that row are left in "stand by" mode. This would significantly reduce operating power to that of operating one module in each row of memory.

Using the system shown in Figures 4-3 and 4-4 and WAROM devices (write time = 2.0 ms), the input data rate to the system is capable of accepting and writing a full saturated write in 1.6 mHz (bit rate). If 8K EAROM's are used in this system the total bit capacity would be extended to 128 megabits but the input data rate would decrease to 320 kHz (bit rate).

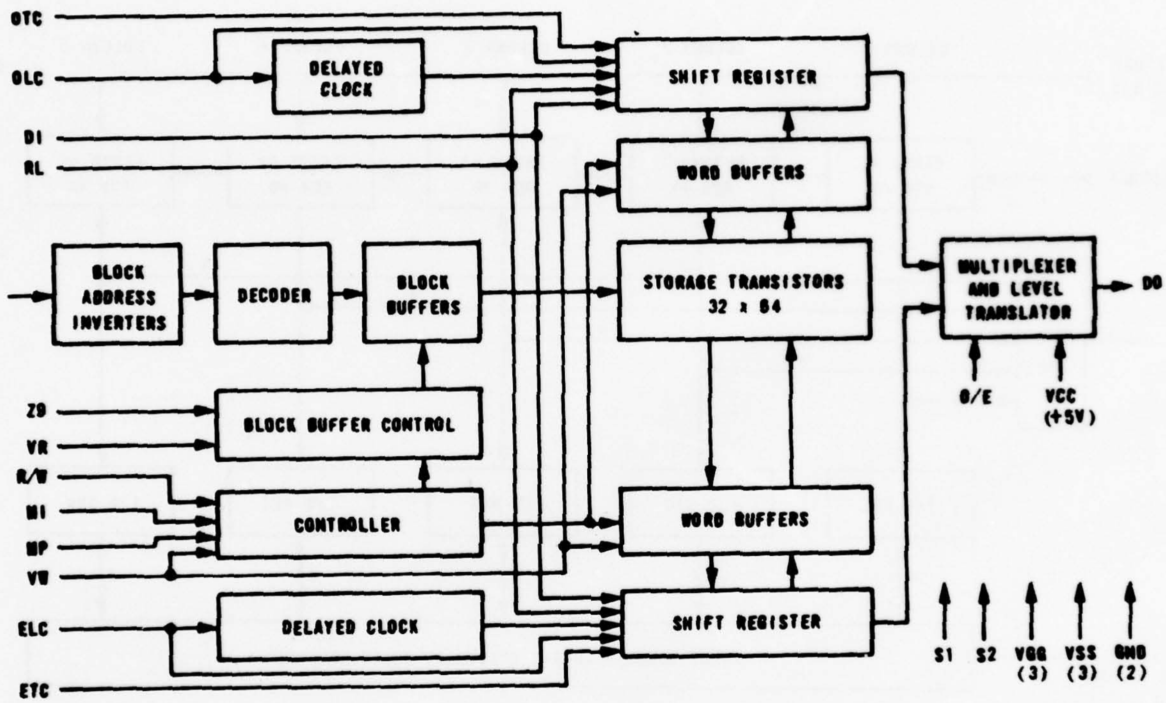

FIGURE 4-1. MNOS BORAM CHIP (2048 BITS)

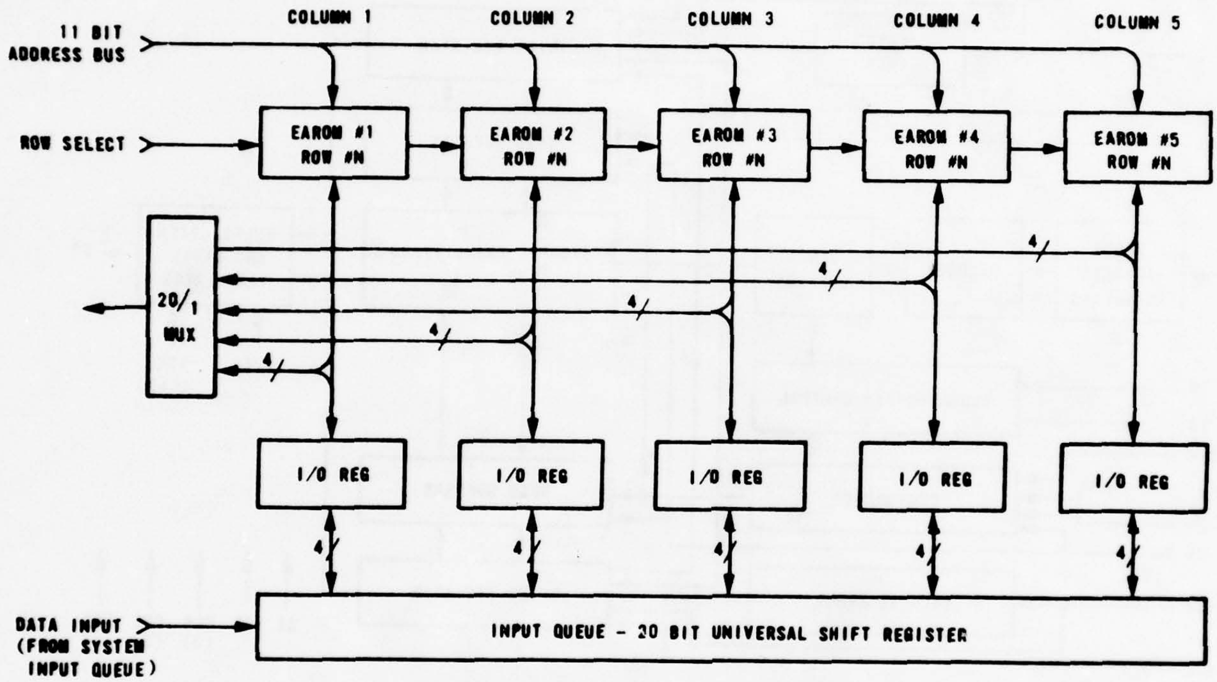

FIGURE 4-2. MNOS BULK MEMORY ROW PAGE
40K WORDS X 1 BIT

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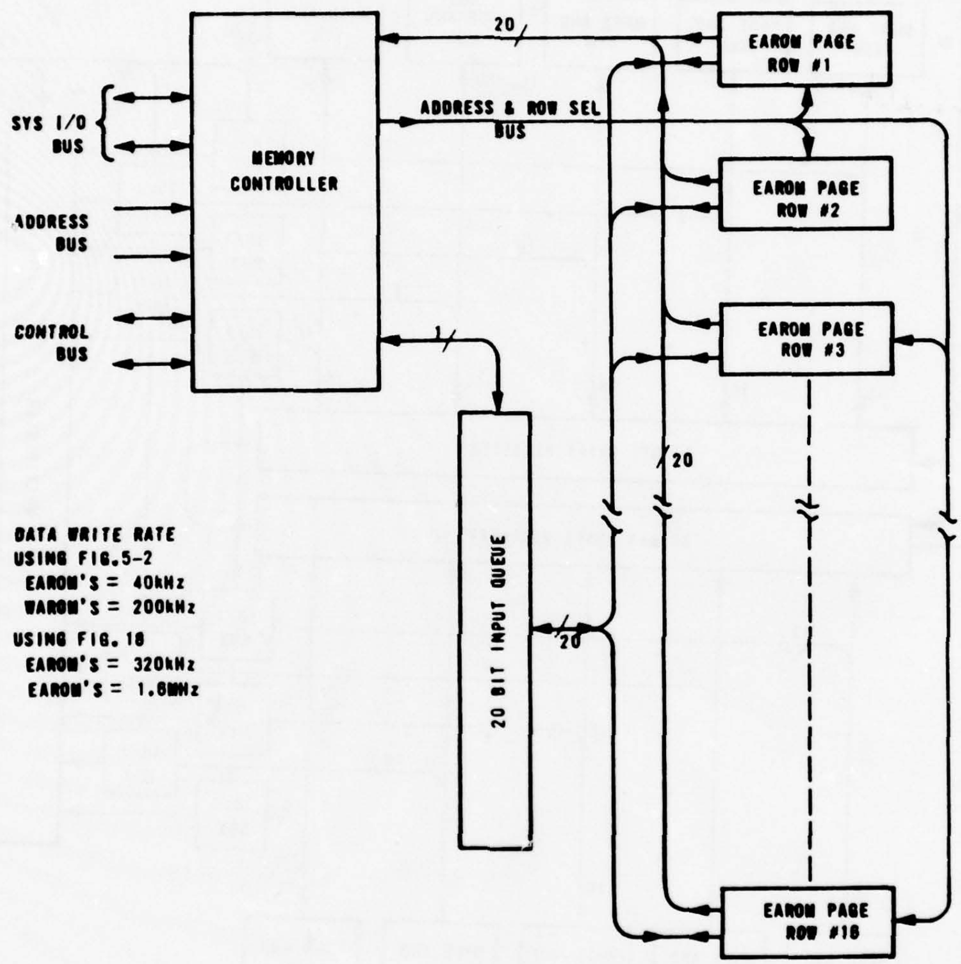

FIGURE 4-3. MNOS BULK MEMORY SYSTEM

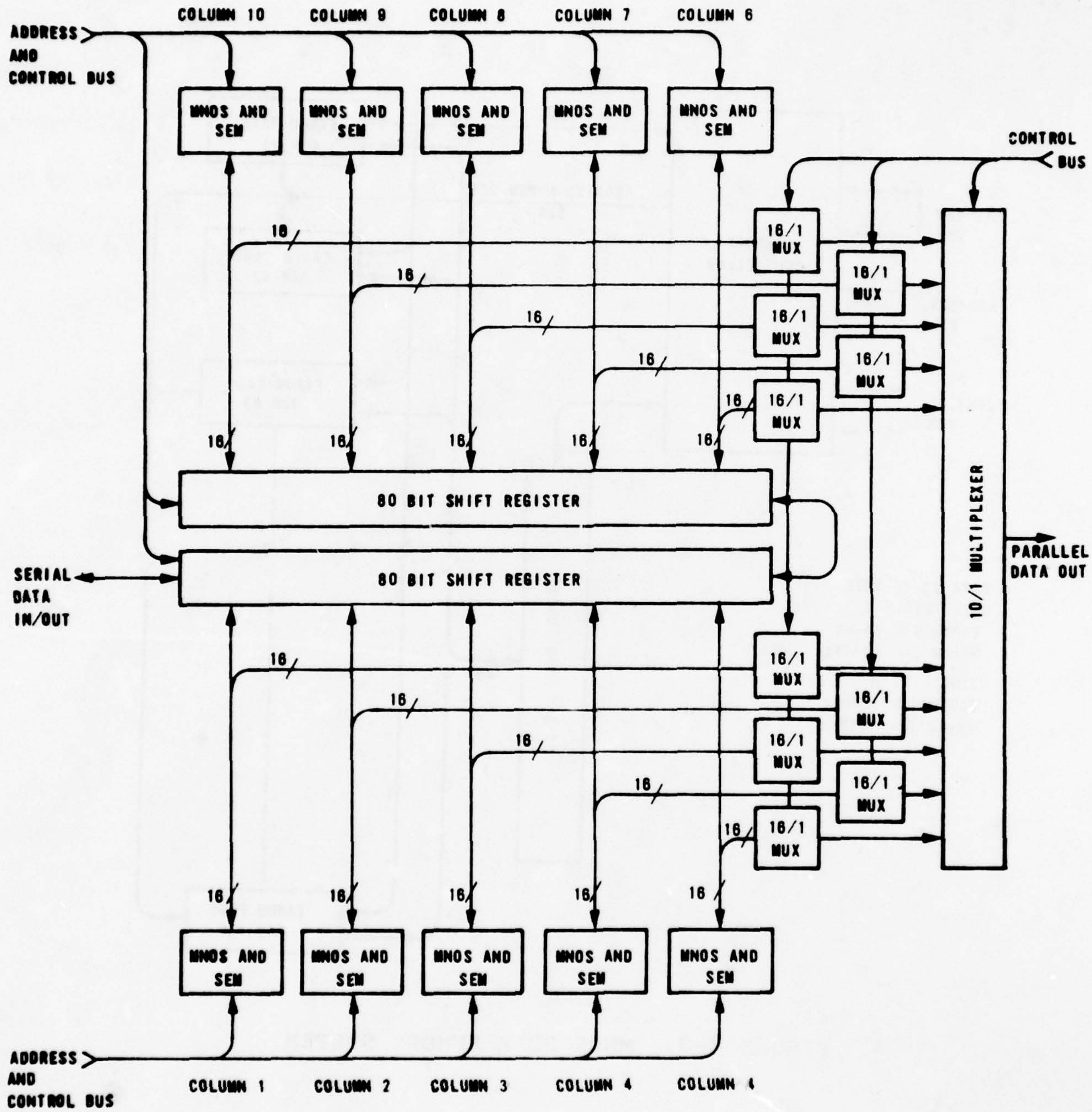

FIGURE 4-4. MNOS BULK MEMORY PAGE USING 320K ISEM MODULE - SYSTEM CAP = 64M BITS

The primary reasons for using WAROMs in this organization is to allow erase of a minimum of four words instead of a minimum of 2048 words which would occur using the bulk erase mode of EAROM's. Since the bulk memory is a serial input memory and the memory controller maps where data is to be placed for assigned tasks, the order and time of required erasure of data can be predicted and implemented in a manner that is transparent to the write mode. By proper data management the new data being input will always be placed in freshly erased sections of memory. The erasure of data will always lead the input of new data such that the oldest data in a file will be the next candidate for erasure.

Using WAROM's groups of words will be erased simultaneously which will not require additional memory to cover the space being erased. Since when using EAROM's such a large section of words are erased simultaneously additional memory may be required. In addition significant sections of a memory file may be lost in a single erasure.

Another organization of WAROM's for use in bulk memory systems is shown in Figure 4-5. This system uses a basic MNOS module illustrated in Figures 4-6 and 4-7 to develop a 64-megabit system using 10 pages of 20 modules each. In this system, the multiplexing and temporary data storage while writing (FIFO's) is performed at the module level. An analysis of the write time using this mode is shown in Table 4-1. On this table, different write times (TW) are assumed for the WAROM. This assumes that "soft" writing is being performed since a reduced retention characteristic is required. The write time versus retention characteristic of the WAROM will follow a curve similar to that illustrated in Figure 4-8.

Another form of bulk memory system using MNOS EAROM's/WAROM's is shown in Figures 4-9 and 4-10. In this system, data rate input buffering is performed in the memory controller FIFO's and the system uses a parallel 16-bit I/O bus to load and read from the memory arrays. Figure 4-9 shows the construction of one page of an eight page system using standard EAROM modules to develop a 64-megabit system. The memory controller shown uses a bit slice microprocessor to control flow and map and dynamically relocate data.

In all three systems shown, data is randomly accessible at the memory system interface in less than two microseconds and power switching modes allow the system to assume the average power of one module per page. Using the first system discussed, the maximum input rate is adjustable by varying the length of the input queue. In the remaining systems, the maximum input rate is fixed depending on the length of the input FIFO's.

MNOS memory offers a reliable bulk memory alternative that features flexibility of approach, microcircuit packaging techniques, repair ability at the box level and fast random access as some of its important features.

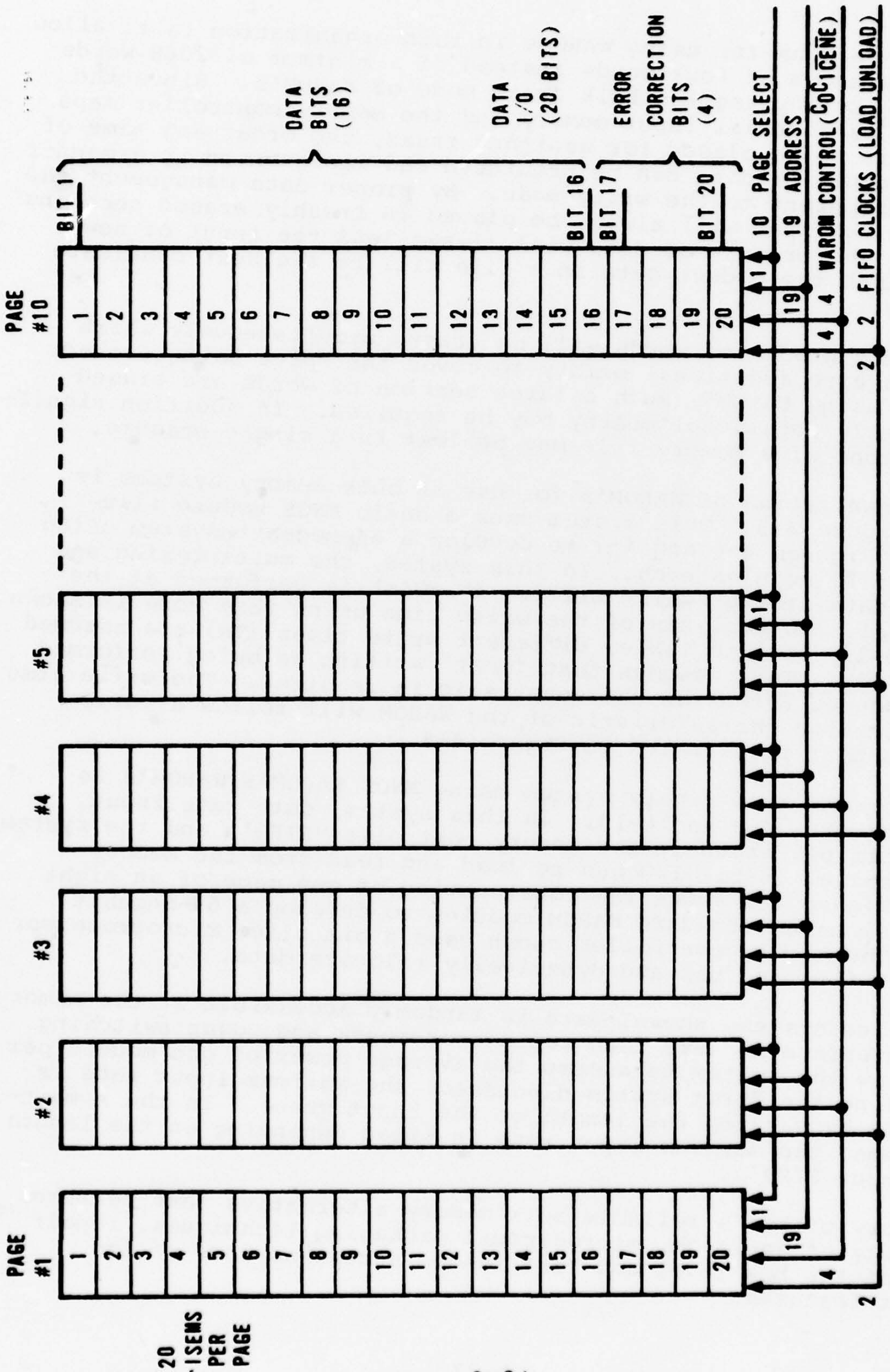

FIGURE 4-5. BULK MEMORY SYSTEM - 64 X 10^6 BITS

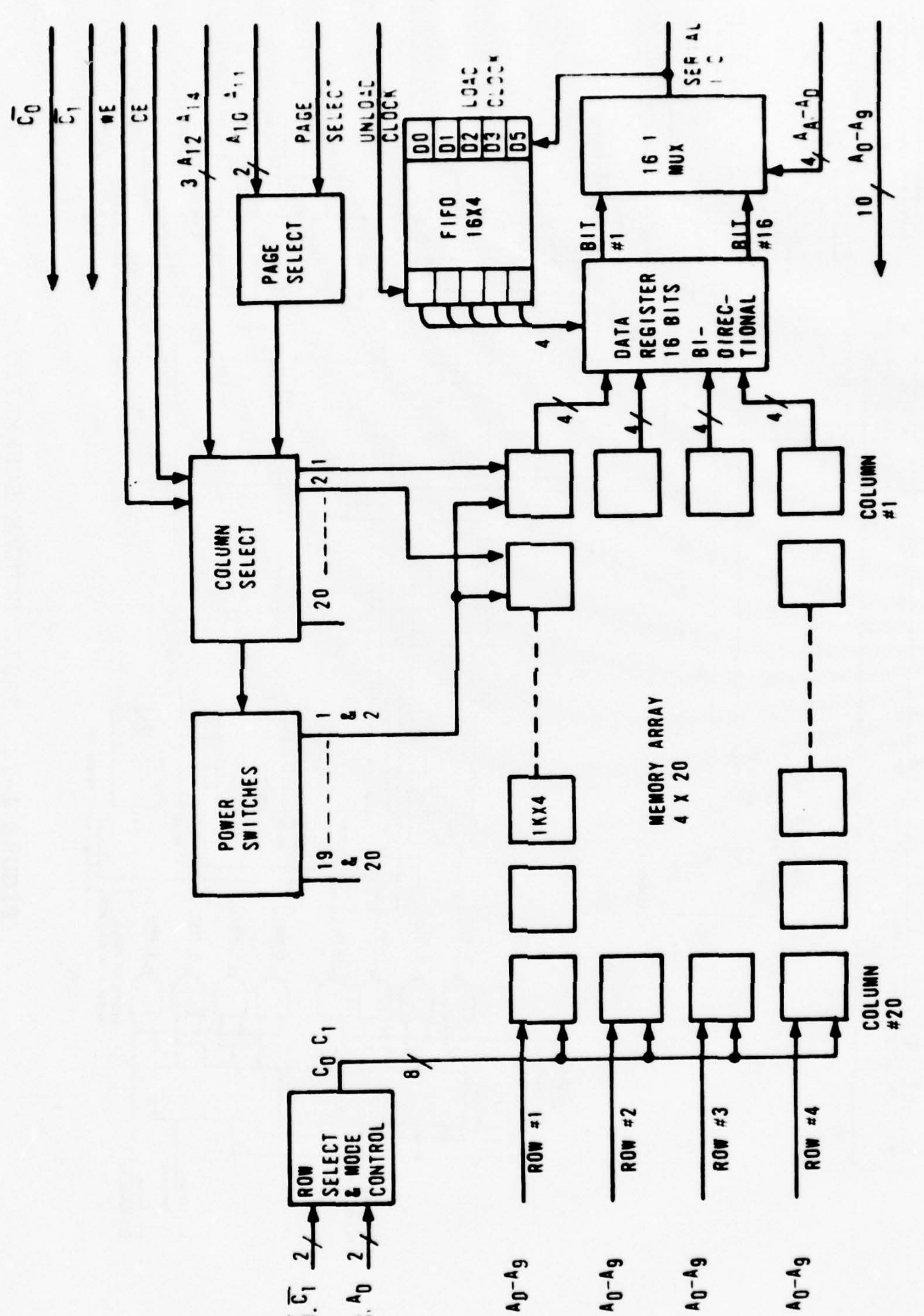

FIGURE 4-6. BASIC MODULE BLOCK DIAGRAM

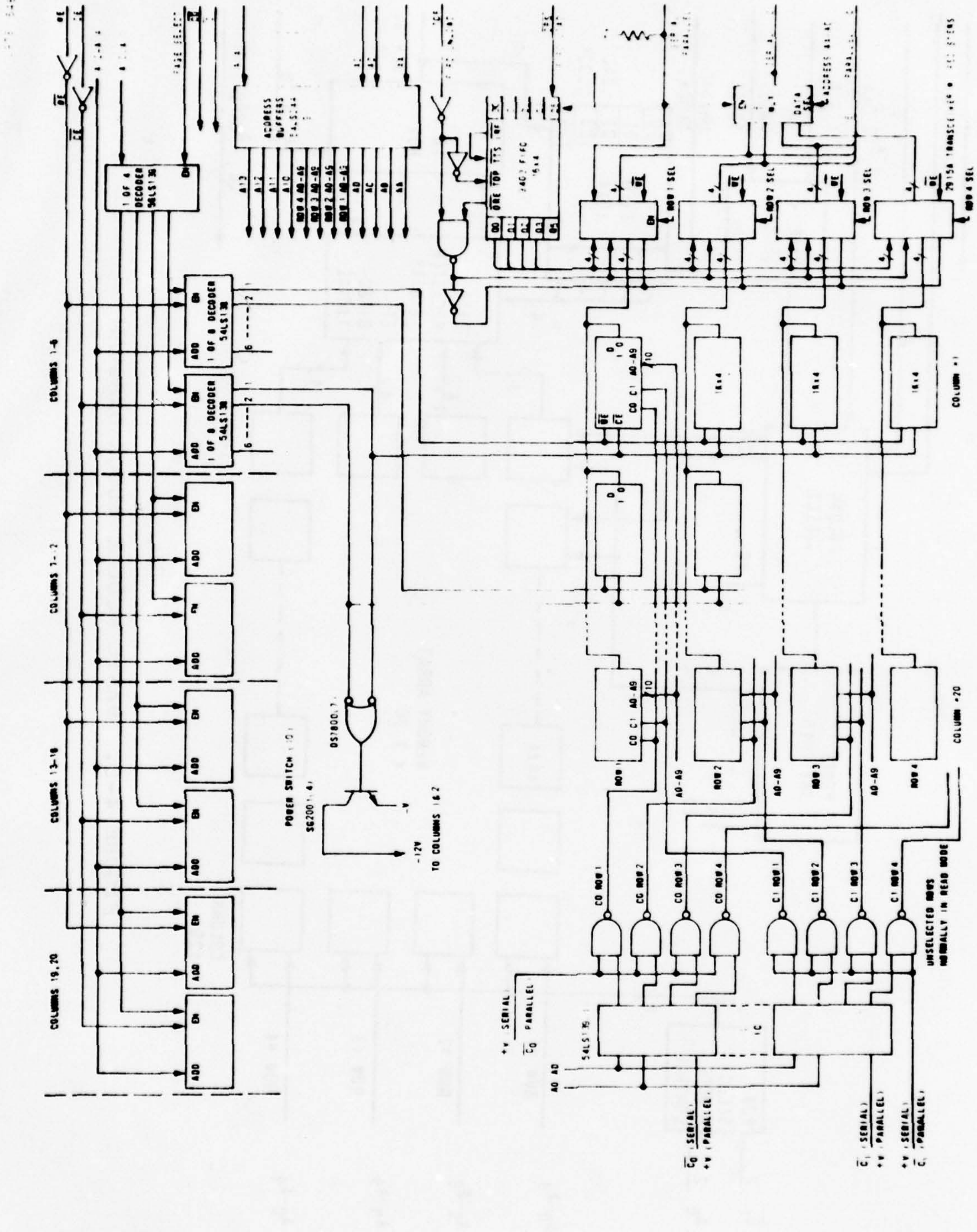

FIGURE 4-7. BASIC MODULE SCHEMATIC

TABLE 4-1. WRITE TIMING ANALYSIS

Serial Input Bit Rate	FIFO Load Time (64 Bits) (μ Sec)	WAROM T_W = 1.0 MS 64 Bits (MS)	WAROM T_W = 1.0 MS Equivalent Bit Rate (μ Sec)	WAROM T_W = 500 ms 64 Bits (MS)	WAROM T_W = 500 ms Equivalent Bit Rate (μ Sec)	WAROM T_W = 100 ms 64 Bits (MS)	WAROM T_W = 100 ms Equivalent Bit Rate (μ Sec)
1.0 mHz (1.0 μSec)	64	16	251	8	126	1.6	26
200 kHz (5.0 μSec)	300	16	255	8	130	1.6	30
100 kHz (10 μSec)	640	16	260	8	135	1.6	35

It is assumed that erase time is transparent, i.e., addresses are erased earlier under program control.

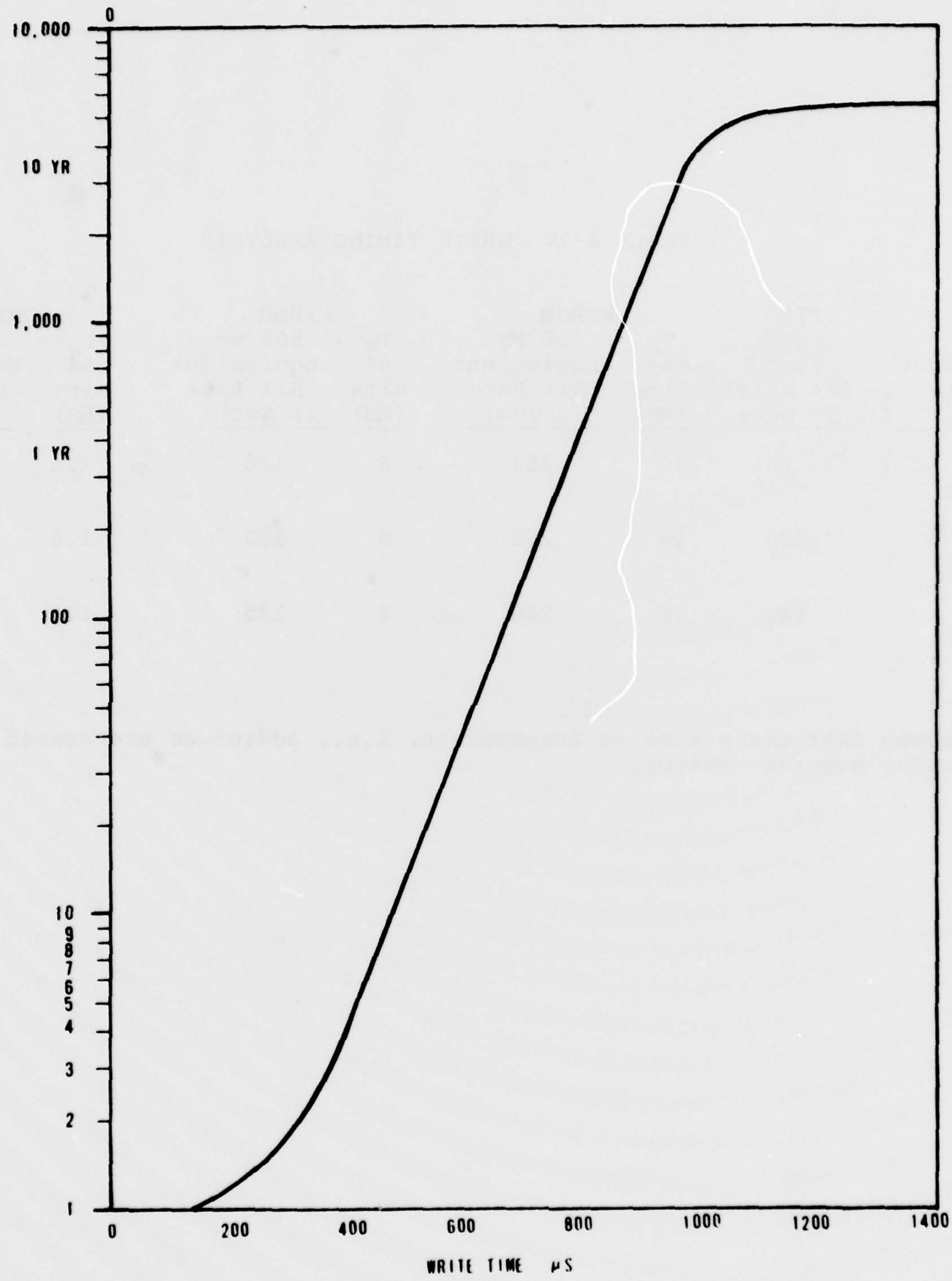

FIGURE 4-8. RETENTION VERSUS WRITE TIME TYPICAL FOR DEVICES OF NCR 2450 (ER 3400/3401)

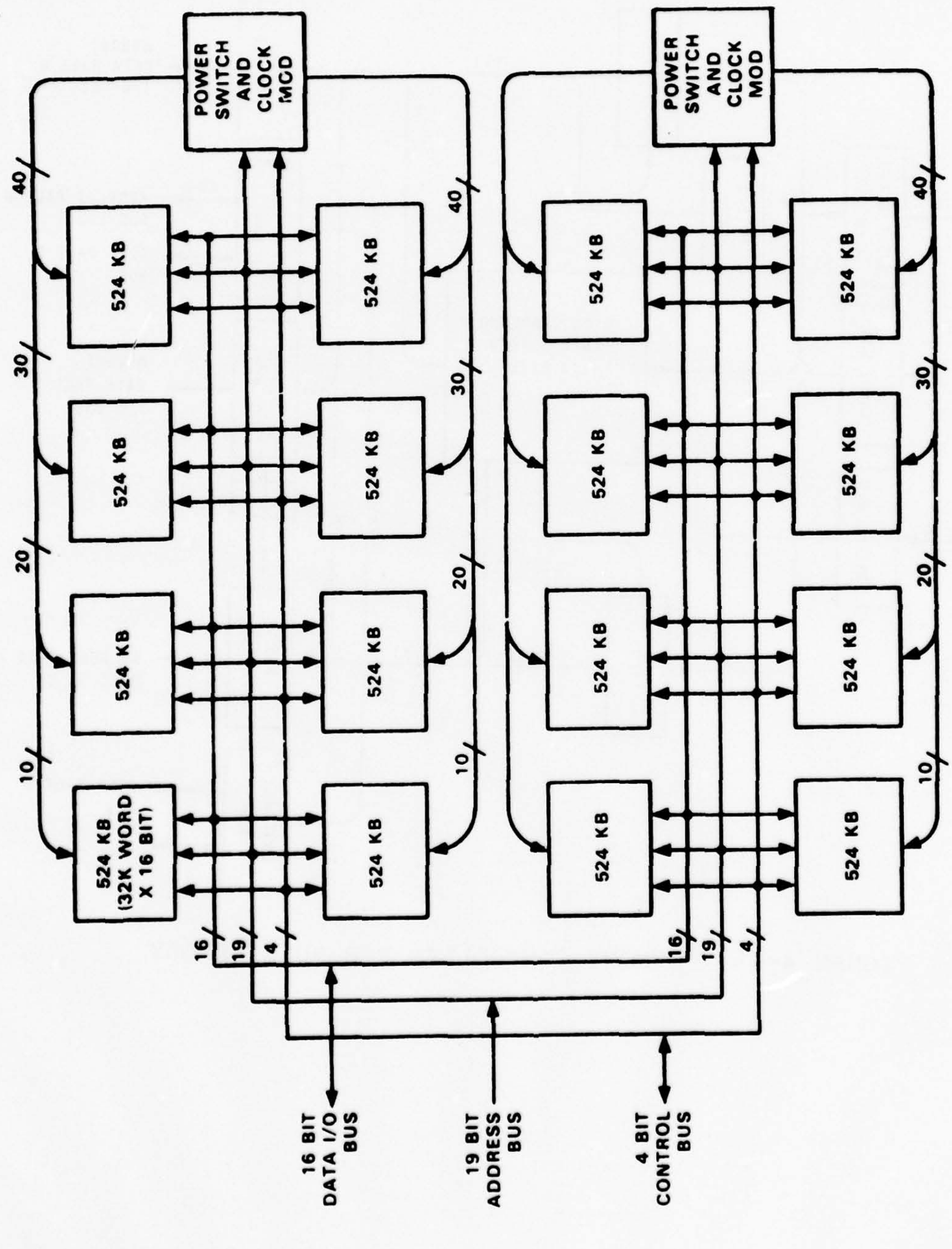

FIGURE 4-9. BULK MEMORY BLOCK DIAGRAM

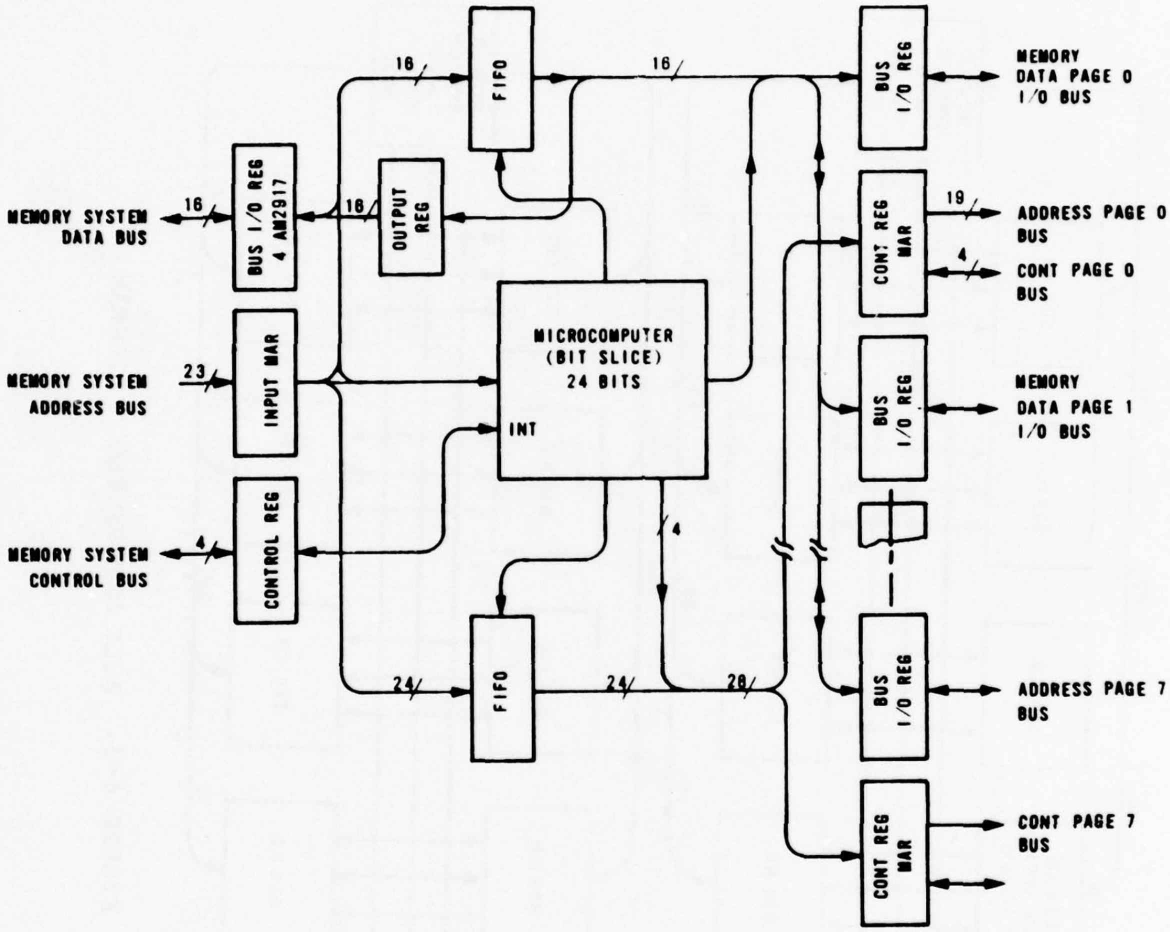

FIGURE 4-10. MEMORY CONTROLLER FOR BULK MEMORY

Section 5

MNOS MEMORY MODULE DEVELOPMENT

The design of any electronic module for use within a military or aerospace functional unit depends upon a number of major factors:

a. Application

b. User and his normal package configurations

c. Size, weight and power restrictions

d. Cost

e. Ease of maintainability

f. The degree of repairability

g. Reliability

At the detailed level, packaging of the module depends upon:

a. Packaging at the circuit level including the chip itself, the dual in-line package (DIP) or the flatpack (FP)

b. The number of allowable module pinouts

c. Power dissipation and its management

d. Parts types and parts count

e. The module housing, frame or carrier

f. The subfunctional package type

If the module under development is a memory module consisting totally of semiconductor devices, then finally module development depends upon the:

a. Storage type - RAM, ROM, EPROM, EAROM

b. Amount of storage (words or bits) required

c. Need for inclusion of non-storage functions such as timing and control, addressing and buffering

d. Necessity for storage only (no support circuitry)

e. Serial or parallel read out

f. Requirement for power switching for power conservation

g. Testability of all memory functions.

Three principal memory module types can be identified. One module type incorporates storage circuits as well as timing, control, addressing and buffer circuit. This module is directly applicable to microprocessor operations as was illustrated earlier in Figure 3-5. The second module type incorporates principally the storage devices with only some circuit buffering included. These modules can serve to expand the storage capability of the first type of module. The third is a module which contains only support circuitry. This final class while the least desirable has some possible system use. The discussion below outlines how these baseline modules can be used in combinations to synthesize larger memories or different package configurations useful in different applications.

The program memory utilized for ATIGS and illustrated in Figure 3-5 is an independent MNOS memory module of the first type alone. Since it was designed for the military environment and, indeed, has been flight tested in this form, it appears to be a candidate for further module development analysis. The dual in-line package version of the 4096-word (with NCR 2401) or the 8192-word (with NCR 2810) is illustrated in Figure 5-1. This modular circuit board contains the 16 MNOS circuit devices necessary to implement the storage. In addition, it contains all timing, control, addressing and buffering circuits illustrated in the diagram of Figure 3-5.

The module of Figure 5-1 is inappropriate for many applications. It is relatively large and bulky and does not take advantage of the small potential size of integrated circuits. For this reason, alternate packaging schemes appear desirable for developing the building block modules for advanced systems where MNOS is applicable. The most desirable circuit packaging candidates reviewed were:

a. Circuit chips mounted on multilayer thick film substrates in turn mounted in hybrid carriers.

b. Circuit chips mounted in leadless carriers in turn mounted on circuit boards or substrates.

The thick film hybrid implementation allows for:

Dense packaging
Good quality control
Potentially low cost (cost per bit)
Good environmental control
High reliability

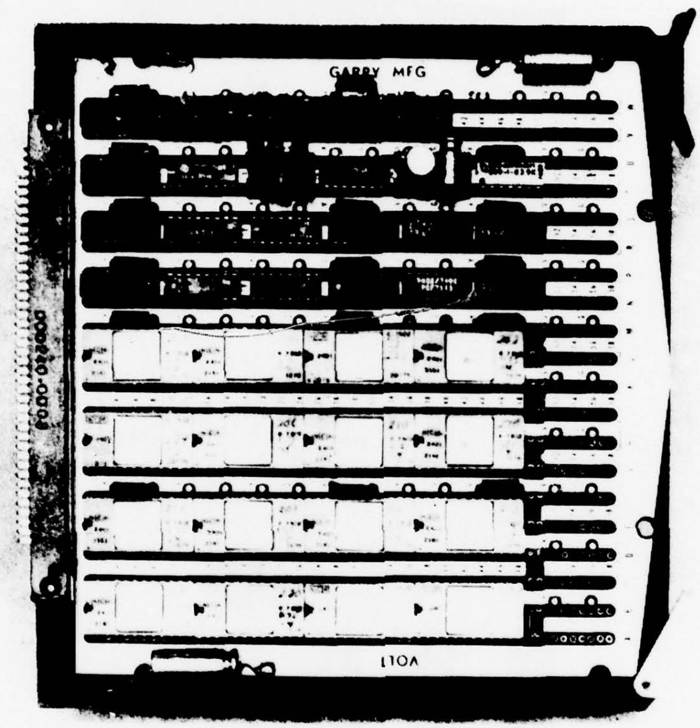

FIGURE 5-1. 4096 WORD MNOS MODULE PACKAGED IN DIPS

The chip carrier implementation (Figure 5-2) is less standard, but still offers dense packaging (less than hybrids) and other advantages over conventional packaging.

The hybrid packaging approach was selected for the ATIGS memory resulting in the configuration illustrated in Figure 5-3. This module incorporates the entire self-contained 4096-(or 8192-) word (16-bit) MNOS memory of Figure 5-1 in a 2 by 2 inch metal housing.

Figure 5-4 further illustrates the hybrid module and in exploded form provides details of its construction.

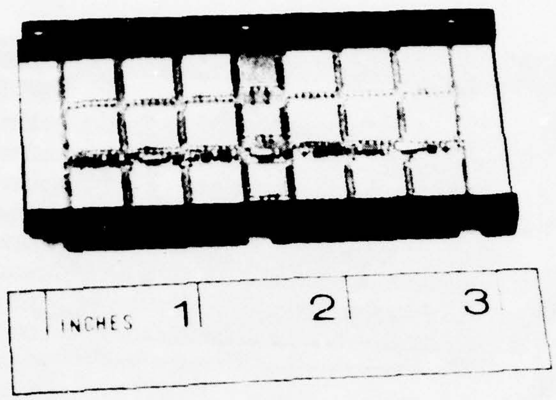

FIGURE 5-2. MEMORY PACKAGED WITH CHIP CARRIERS

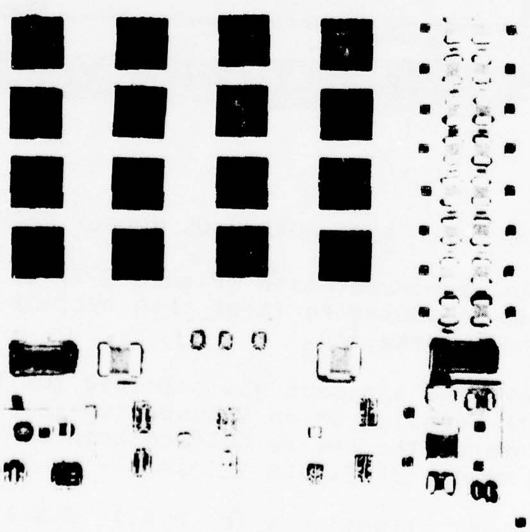

FIGURE 5-3. MNOS HYBRID MODULE

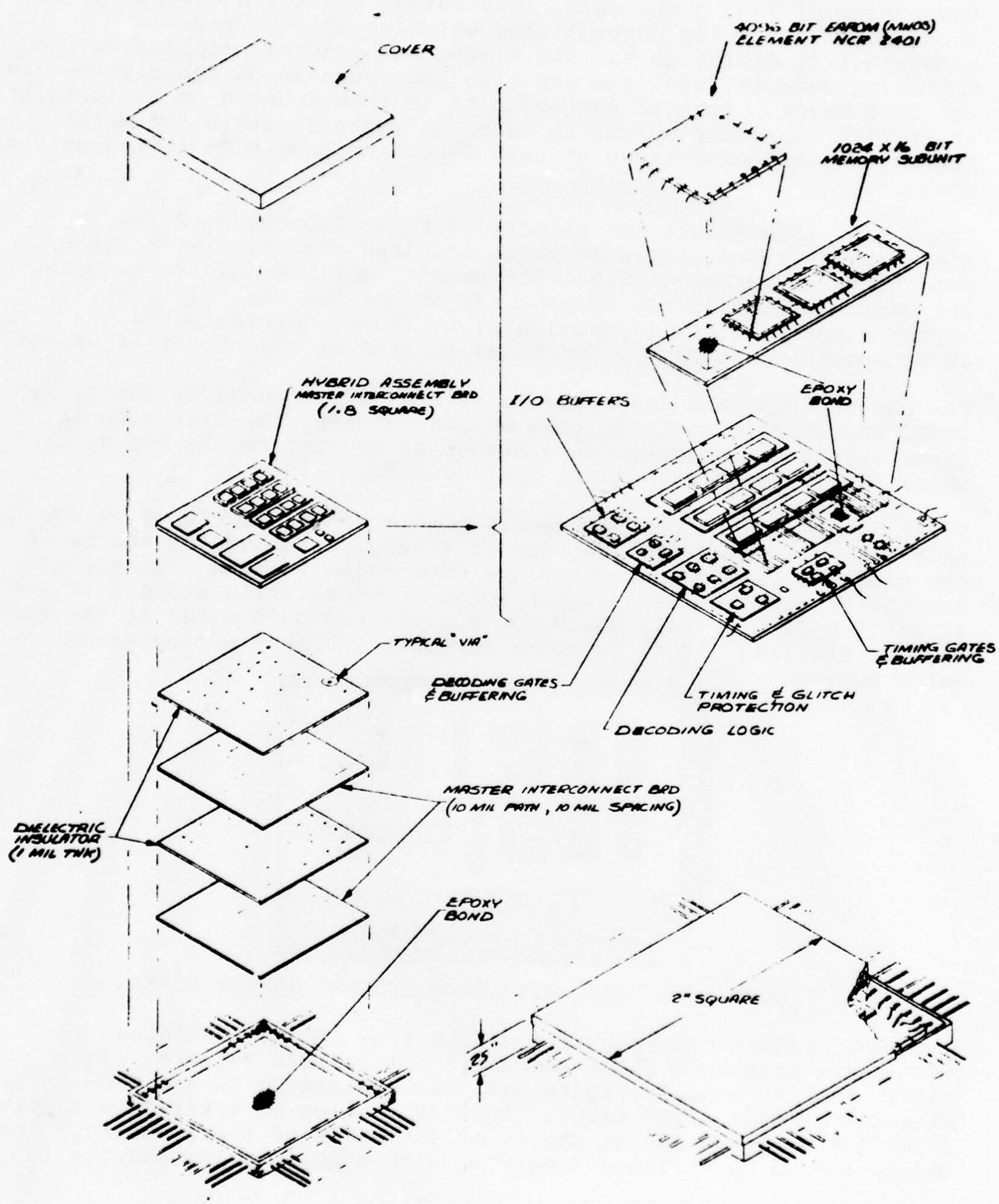

FIGURE 5-4. 4096 WORD MNOS MODULE

SYSTEM CAP = 64M BITS

A-22

The 2 by 2 inch structure contains 16 MNOS chips arranged in submodules of four chips each. Pretesting (static and dynamic) of these subunits can be accomplished which greatly improves the producibility of the unit. The timing and control, addressing, and buffering circuit functions are also incorporated on subunits as are the MNOS chips. Each of the subunits is then mounted on a six-layer thick film substrate which, in turn, is mounted within the metal housing. Interconnections at each level are made with flying gold wires.

The 2 by 2 inch module was selected for ATIGS because of the similarly packaged processor which required the relatively large periphery for pinouts. Since the memory requires much fewer pinouts the 2-inch hybrid is not necessarily an optimum one. In fact, it appears that a 1-inch (approximate) by 2-inch (approximate) can accommodate enough memory functions to make it a cost effective size.

For our hypothetical development, herein, if we consider the proven ATIGS module as a baseline then we can consider the five subunit types as building blocks for a number of revised module types from which larger functions can be synthesized.

First, a standalone program memory module can be developed as shown in Figure 5-5 which includes the four support submodules and two of the memory array submodules (eight MNOS chips). Such a module can provide as much as 2048, 16-bit words of nonvolatile storage if the 4K bit NCR 2401 or 2431 WAROM is utilized and 4096 words if the NCR 2810 is utilized. This is quite adequate for many microprocessor based systems.

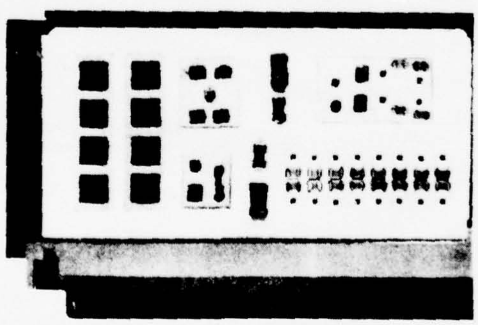

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FIGURE 5-5. 4096-WORD MNOS PROGRAM MEMORY HYBRID

A second program memory hybrid module type can be developed containing only MNOS chips and their appropriate buffers. This highly regular module (Figure 5-6) can contain up to six MNOS array submodules (four chips each). This collection of arrays can supply up to 12K words of 16-bit memory or 24K words of 8-bit memory. This module should be utilized singly or with other similar modules to

extend the storage associated with the first type of module. For example, with one module of the first type and one of the second type as much as 16K words of 16-bit storage can be provided.

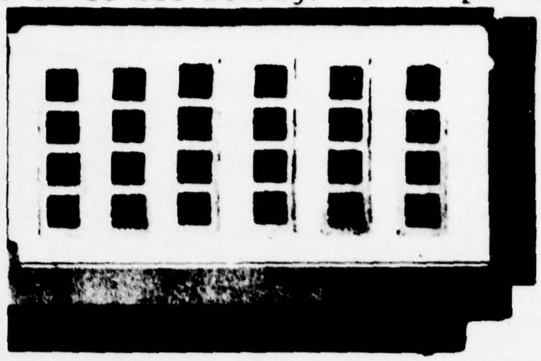

FIGURE 5-6. 12288/6144 WORD MNOS HYBRID MODULE

A third hybrid memory module type is a reduced version of the first and would contain only support circuitry subunits. Such a module will not be discussed herein, but does have the advantage of isolation of the support circuitry from the MNOS arrays. This approach to module design would accommodate technology changes in MNOS devices without change to the base module design. It does not provide as high a packing density as the other module designs however.

Once the first two module types are developed, they provide versatile building blocks for many physical configurations. Figure 5-7 illustrates how the basic hybrid modules can be included on circuit boards in conventional (ATR) aircraft package configurations. It further illustrates how these modules are included on the unconventional assemblies associated with missile and torpedo configurations. Finally, it illustrates how the modules can be included in combinations on the Navy's SEM, SAM, or ISEM configurations. These standards readily accommodate 1 by 2 inch hybrids in the numbers required for the total storage needed.

Figure 5-8 illustrates a possible ISEM configuration which can be used as both a program memory and as a replicated building block for large bulk storage systems. The module can be assembled from the 1 by 2 inch hybrid modules discussed in a previous paragraph. In this configuration, it can be used singly in conjunction with a microprocessor assembly. A number of these can implement the bulk memory discussed in the previous section.

The ISEM module just described used proven circuits, proven subunit designs and conventional circuit assembly techniques. This proven approach provides a relatively dense memory module which is more than adequate for the general purpose processor program memory. For the

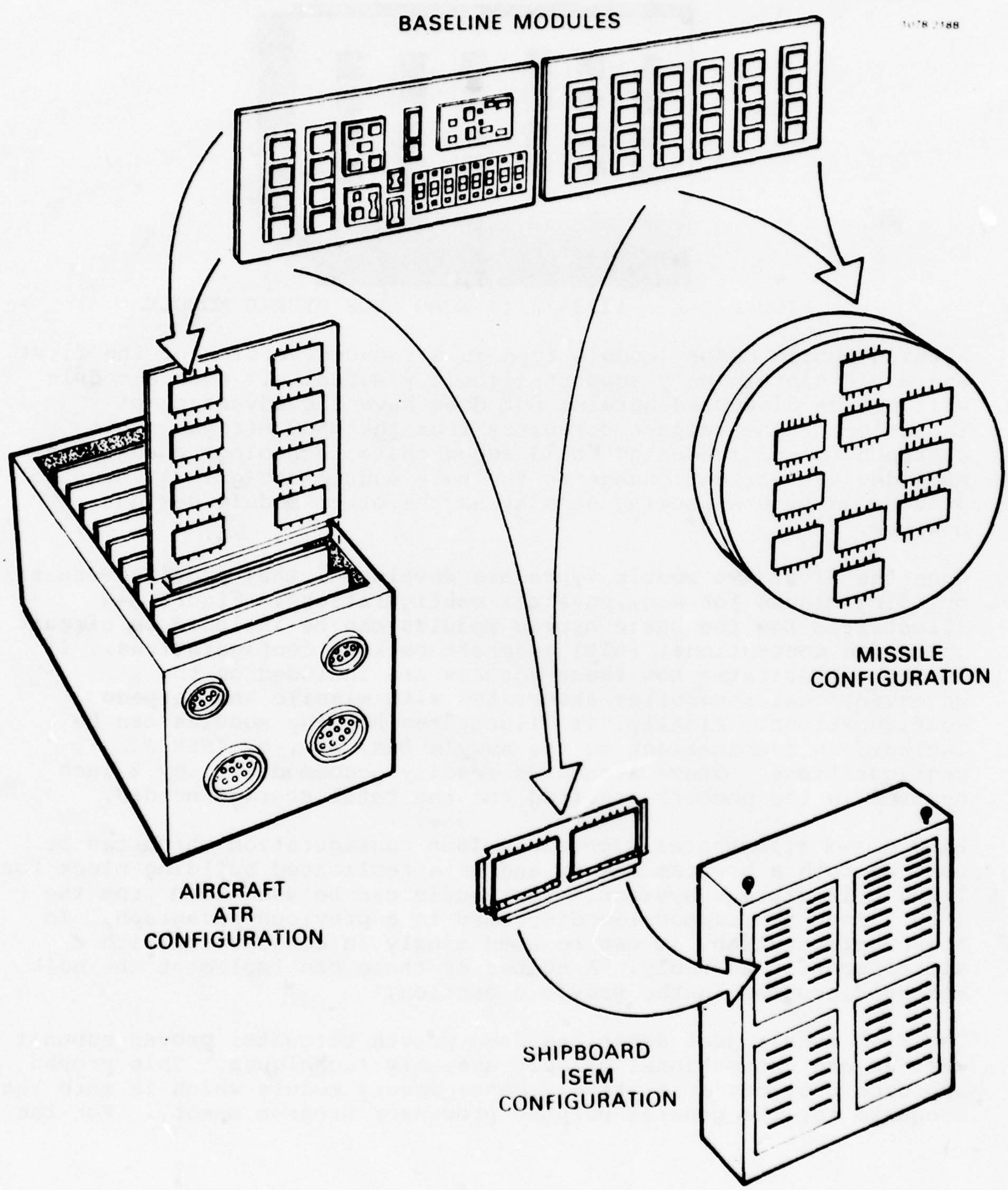

FIGURE 5-7. APPLICATION OF BASELINE MNOS MODULES

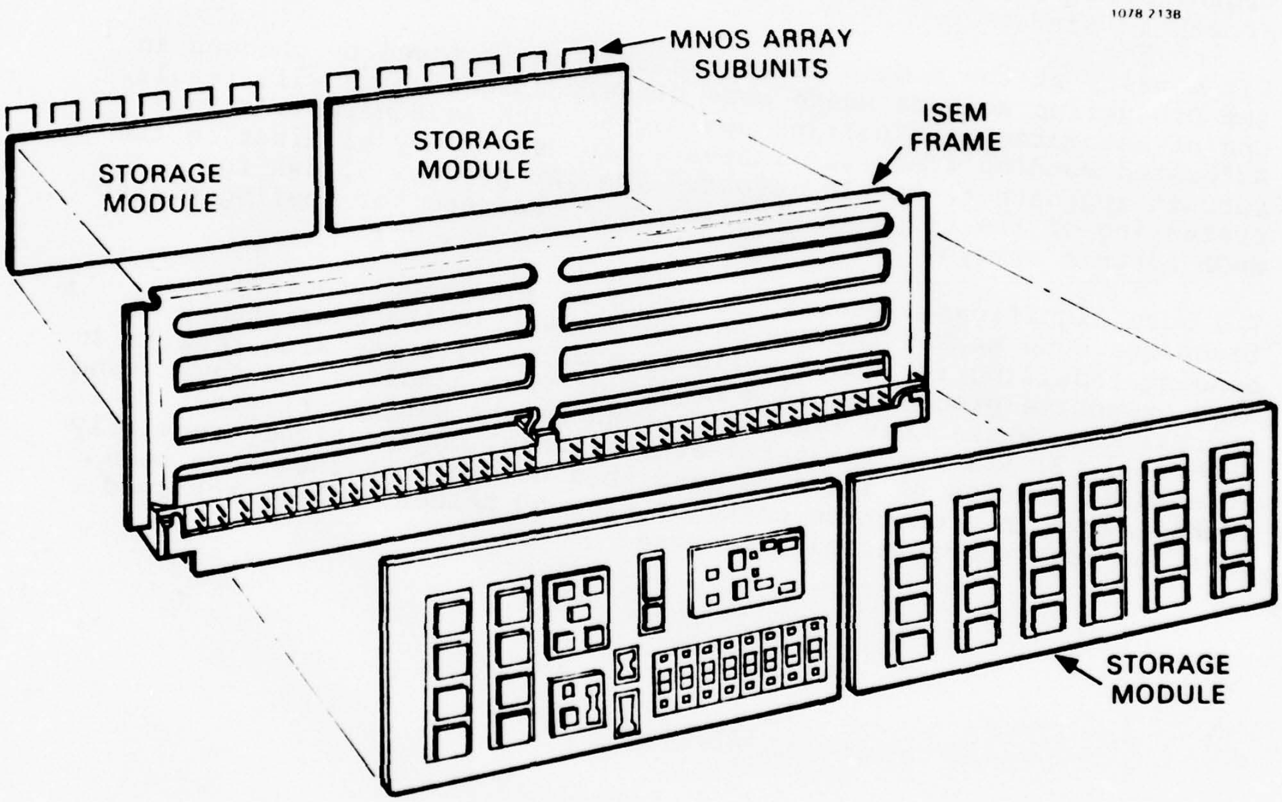

FIGURE 5-8. 655K BIT MNOS MEMORY MODULE

bulk memory, however, several improvements or alternate approaches should be taken to effect more dense word alterable storage at a lower per bit cost.

The density of MNOS EAROMs (presently 8K chips) and WAROMs (presently 4K chips) are expected to double within the next 3 to 5 years. This doubling of bit density at the chip level doubles the bit density at the module level with little increase in the power dissipation. Also, most density improvement in the chip has seen few chip organization changes which means that module layouts can keep density growth in mind.

Bit density at the module level can also be improved by changes in the production methods where more closely spaced chips will result. Use of automated-type carrier approaches such as Honeywell's Tape Automated Bonding (TAB) can increase the density by eliminating the subunit approach to module layout. The TAB process allows for pretesting of the chips which eliminates the need for testing of the MNOS subunit arrays.

The more significant reasons for using an automated processing technique such as TAB include an improvement in the consistency of bonding resulting in a more reliable module. Its use also results in less expensive processing as a result of less handling and fewer hand operations. While this type of process is the subject of other papers (1, 2) its use is worthy of consideration for highly regularly structured modules of the type described herein. Savings have been demonstrated in production costs of over 50 percent can be achieved over the more conventional processes.

Section 6

CONCLUSIONS

This paper has attempted to describe the potential application areas of MNOS EAROMs and WAROMs. In particular, program memory and bulk memory functional configurations are illustrated which describe practical applications of the MNOS devices. Finally, physical modules are configured which can be used in either program memories or bulk memories.

MNOS growth started slowly and now is expanding rapidly especially for commercial users. The next few years will see rapid advances which are particularly useful in developing MNOS mass memories which are competitive with disk devices.

While MNOS memories at the present time are made in 8K bit EAROM and BORAM devices and 4K WAROM configurations all of these are constructed using P channel MOS technology. Due to the 3 to 1 mobility difference between N and P channel devices most new research is being directed toward developing N channel devices. This should result in MNOS memories with access times compatible with the new MOS microprocessors and make the memory organizations optimum for use in these applications.

The remaining MNOS development effort has been directed toward designing devices with on-chip voltage multipliers to allow single low voltage operation and the design of NVRAMs (Non-Volatile Random Access Memories). The device using voltage multipliers are designed to allow write/erase operations as well as read using voltages typical of microprocessor operation (+5V, -15V) since these operations are low current modes the approach is entirely feasible.

The development of Non-Volatile RAMs will allow these devices to operate in the write mode (no erase necessary) at computer speeds. Each volatile RAM cell contains a non-volatile MNOS transistor which is written only when a "store" pulse is issued when the power begins to go down. In this manner the advantage of non-volatility of data is added to the fast RAM operation. This approach also enhances the life potential of the MNOS cell since it is only written when the power is removed which minimizes the endurance (i.e., wear-out) characteristic.

The predicted level of development in MNOS devices is shown in Table 7-1.

With these advances in MNOS Memory Technology will come improvement in the endurance and retention characteristics and reduced power consumption. MNOS looks like it may replace many of the present memory technologies in the military market.

TABLE 6-1. MNOS DEVICE DEVELOPMENT TRENDS

1978 — 1979 — 1980

1. Device Capacity
   #/Bits
   - P Channel: 8K → 16K
   - WAROM: 4K → 16K →
   - N Channel: 1K → 4K → 16K → 65K

2. Access Time
   Nano Seconds
   - P Channel: 650 → 500; 1400 → 900 → 800
   - N Channel: 600ns → 400ns → 200ns

3. Organization
   - P Channel: 2K x 4 → 2K x 8; 1K x 8
   - N Channel: 256 x 4 → 512 x 8/1K x 4 → 2K x 8/1K x 16 →

4. Radiation Hardness
   # RADS
   - P Channel: 10^5 → 5×10^5
   - N Channel: 1×10^4 → 10^5 → 10^6

5. Cost/Bit
   Cnts/Bit
   - P Channel: .3 → .2 → .1
   - N Channel: 2.0 → 1.0 → .5 → .25

6. Write/Erase Time
   micro Sec
   - P Channel: 10K → 1K
   - RAMS: 100 → 10 → 2 → 1µs
   - N Channel: 10K → 1K → 200 → 10

Section 7

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2. "The Evolution of the MNOS EAROM and its Application to Avionics and Other Military Systems", C.E. Collum, R.L. Wiker and W. Spence, paper presented at NAECON Conference, 1975.

3. "A Minicomputer Adapted to Tactical Missile Guidance and Control", C.E. Collum and O.E. Marvel, Internal Honeywell Paper, 1975.

4. "Technology Trade-offs in Deriving the ATIGS X-0 ADCS Configuration", C.E. Collum, Internal Honeywell Paper, 1975.

5. "Design to Cost of a Tactical Missile Guidance and Control Computer", C.E. Collum and W.C. Cross, presented at American Defense Preparedness Assoc., 1975.

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Attachment B

MNOS MILITARY APPLICATIONS SURVEY

This list of questions is designed to determine both the need for and types of MNOS Electrically Alterable Read Only Memories (EAROM's) suitable for military/aerospace applications. The results of this survey will be used as one of the criteria for selecting which commercially available MNOS device will be used in a program instituted by the U.S. Army ERADCOM Electronics Technology and Device Laboratory at Fort Monmouth, N.J. called MACI (Military Adaptation of a Commercial Item). The object of this program is to select from a number of candidate MNOS devices one which is most suitable for Military Applications and develop suitable screening tests and qualification data to submit the device for military qualification. Honeywell is performing this program for the Army.

INTRODUCTION

The intent of these questions is to determine the potential applications of EAROM's in military systems, the optimum memory device organizations and characteristics for these applications and the characteristics and/or organizations desireable for future use.

There is no intent in this program to analyze or investigate optimum organizations for devices other than EAROM's. Other acronyms for EAROM's include:

a. AROM - Alterable Read Only Memory
b. EPROM - Electrically Programmable Read Only Memory
c. WAROM - Word Alterable Read Only Memory

These organizations are included in the program.

While BORAM's (Block Oriented Random Access Memories) and SAM's (Serial Access Memories) overlap the applications areas of EAROM's, investigation of optimum organizations for these devices is left to other programs.

QUESTIONS

1. Does your organization use or intend to use MNOS EAROM's in your systems? YES NO .

2. Which of the following types of systems most closely describes your application? (Circle)

   (a) Data Processing/Program Storage

   - Large Main Frame
   - Minicomputers
   - Microcomputers

   (b) Data Acquisition

   - Disc Replacement
   - Tape Replacement
   - Special Environment

   (c) Read Mostly Memories

   - Character Generators
   - Look-up Tables
   - Map Storage

   (d) Bulk Memory

   - Disc Replacement
   - Core Replacement
   - Special Environment

   (e) Controller Applications

   - Microcode Memory
   - Instruction Memory
   - Code Generators

3. Which of the following MNOS EAROM characteristics is most attractive to you for use in your system? (Assuming non-volatility is required.) List from 1 to 9

   (a) High Density

   (b) Low Cost (Approx. 0.25¢/Bit)

   (c) Fast Random Access

   (d) Instant Bulk Erase (Secure Erase)

   (e) Electrical Write and Erase

   (f) Capability of Use in Hybrid Package

   (g) Low Power (i.e., Low Active or Standby Power)

(h) Radiation Resistance

(i) Other ____________________

4. What is the preferred number of bits per word on chip in your system for a MNOS device?

   (a) 1

   (b) 2

   (c) 4

   (d) 8

   (e) 12

   (f) 16

   (g) Other ____________________

5. What is the preferred MNOS memory device organization for your system?

(a) 64 x 16	(g) 1024 x 4
(b) 256 x 4	(h) 1024 x 8
(c) 256 x 8	(i) 1024 x 16
(d) 256 x 16	(j) 2048 x 4
(e) 512 x 4	(k) 2048 x 8
(f) 512 x 8	(1) Other ____________________

6. Of the following device features listed (a thru z) match the feature with the level of importance to you in applying MNOS to your system. (c) Critically important; (s) significant; (d) desirable, but not important; (I) Irrelevant to your application; (u) undesirable, but not prohibitive; (p) prohibitive for use in your systems.

   (a) Memory Transistor threshold testability (for retention prediction).

   (b) Single Chip Select

   (c) Double Chip Select

   (d) Quadruple Chip Select

(e) Programmable Chip Selects

(f) TTL I/O Compatibility on all inputs and outputs (Including clock)

(g) Clock (where applicable) amplitude +5 vdc (VIH) to -23V (VIL)

(h) CMOS I/O compatibility on all inputs and outputs (including clock)

(i) Fast read access time ($\leq$500 ns)

(j) Medium speed read access time ($\leq$1 μs)

(k) Memory status output (output valid indicator)

(l) Single power supply operation

(1) VSS = +5 vdc ±5%
(2) VSS = 0 to +10 vdc ±10%
(3) Other ________________

(m) Double power supply operation

(1) VSS = +5 vdc ±5%
VDD = 12 vdc ±5%
(2) VSS = 5 vdc ±5%
VDD = -30V ±5%
(3) VDD = 9.0 vdc ±10%
VP = 30 vdc ±5%
(4) Other ________________

(n) Triple power supply operation

(1) VSS = +5 vdc ±5%
VM = -5 vdc ±5%
VDD = 14 vdc ±10%
(2) VSS = 5 vdc ±5%
VDD = 12 vdc ±5%
VGG = -30 vdc ±5%
(3) VCC = +5.0 vdc ±5%
VDD = -15 vdc ±5%
VSS = ±15 vdc ±5%

(o) Data Retention Time

(1) $\geq$1 minute
(2) $\geq$1 hour
(3) $\geq$24 hours

(4) >6 months
(5) >1 year
(6) >3 years
(7) >10 years

(p) Read Disturb Retention

(1) $>10^6$ Reads
(2) $>10^9$ Reads
(3) $>10^{12}$ Reads
(4) $>10^{16}$ Reads
(5) Other ____________

(q) Switched Power Supply Operation

	Read	Write	Erase
Vad	-14 vdc	-23 vdc	+5 vdc
Vm	-5 vdc	-23 vdc	+5 vdc
Vss	+5 vdc	+5 vdc	+5 vdc
VO_1 (clk)			
VIH	+5 vdc	+5 vdc	+5 vdc
VIL	-14 vdc	-23 vdc	

(r) Cost per Bit

(1) 2¢/Bit
(2) 1¢/Bit
(3) 0.5¢/Bit
(4) 0.25¢/Bit
(5) 0.1¢/Bit
(6) 0.01¢/Bit

(s) Number of write/erase cycles before wear-out (endurance)

(1) 10^3
(2) 10^4
(3) 10^5
(4) 10^6
(5) 10^8
(6) 10^{10}
(7) 10^{12}
(8) 10^{15}
(9) Other ____________

(t) Nondestructive Read Out (NDRO)

(u) Dual In Line Package (DIP) size

(1) 16 Pin
(2) 18 Pin
(3) 20 Pin
(4) 22 Pin
(5) 24 Pin
(6) 40 Pin
(7) Other ____________________

(v) Flat Pack

(1) 16 Pin
(2) 20 Pin
(3) 24 Pin
(4) 40 Pin
(5) Other ____________________

(w) Temperature Range

(1) 0 to +50°C
(2) 0 to +70°C
(3) -20°C to +70°C
(4) -20°C to +85°C
(5) -55°C to +70°C
(6) -55°C to +85°C
(7) -55°C to +95°C
(8) -55°C to +110°C
(9) -55°C to +125°C
(10) Other ____________________

(x) Word Erasability

(y) Bulk Erasability

(z) Other Features ______________________________

7. Of the following MNOS devices which have you used or are you planned to use in future systems?

(a) NCR/GI 2401

(b) NCR/GI 1711

(c) NCR/GI 2805

(d) NCR/GI 2801

(e) NCR 2451 / GI 3401

(f) GI 3400

(g) NITRON 7040

(h) NITRON 7050

(i) NITRON 7050

(j) NITRON 7053

(k) NITRON 7054

(l) Other ______________________

8. Is power consumption a major criteria for use of MNOS devices?

   YES NO

9. If answer to (8) is yes, which of following is acceptable for use in your system?

   (a) 100 mw for 4K bits

   (b) 200 mw for 4K bits

   (c) 500 mw for 4K bits

   (d) 300 mw Active - 50 mw Standby for 4K bits

   (e) 500 mw Active - 50 mw Standby for 4K bits

   (f) 100 mw Active - 0 mw Standby for 4K bits

   (g) 300 mw Active - 0 mw Standby bits

ATTACHMENT C

THRESHOLD MEASUREMENT PROCEDURE

MNOS memory depends upon charge trapping at the silicon oxide/silicon nitride interface of the gate insulation region. This trapped charge directly influences the threshold voltage of the storage transistor. The storage transistor threshold is translated into a binary output by a latching differential amplifier. One differential input is connected to the drain of the selected storage transistor through decoding circuitry and the other input depends upon the device.

In the 2810/2401 EAROM, the second differential input is normally supplied by an erased reference MNOS transistor. To measure threshold, V_R is switches from V_{SS}-20 to V_{SS}, and the second differential input comes from a voltage divider at approximately V_{SS}-3. In the 2451/3400 WAROM, the second differential input is always supplied by a voltage divider.

In the 2810/2401 the V_m voltage is applied to the gate of the selected storage transistor (with an offset across the switching circuitry). In the 2451/3400 the gate voltage is normally supplied by a voltage divider. This is called the reference voltage and can be measured on pin C_I by switching pin C_O to V_{gg} (-30V). In the threshold measurement mode ($-15V < V_{gg}$), V_{gg} is applied through switching circuitry directly to the gate of the selected storage transistor. The device must be read several times before V_{gg} is applied to the gate.

Once in the threshold measurement mode, the selected storage transistor can be measured by repeatively clocking the device while slewing V_{gg} (2451/3400) or V_m (2401/2810). The voltage at which the output of the differential amplifier changes state is the threshold of the cell.

With large arrays of cells, the procedure is to measure the least negative threshold of the written cells ("0" threshold) and the least positive of the erased cells ("1" threshold). This is done by reading the device at a voltage between the forementioned thresholds. If the data of all addresses matches the data used to write the memory, the voltage is decreased by 0.02V and again tested. When the "0" threshold is reached (a programmed zero reads as a "one"), the voltage of the last successful test is printed out via teletype and used as V_{TO}.

The procedure is repeated to find the "1" threshold. In this case, the voltage is increased by 0.02 volt following each successful test when the threshold is reached (a programmed one reads as a zero), the voltage of the last successful test is printed out via teletype and used as V_{TI}.

In this procedure, it is critical that the initial voltage be within the threshold window defined by V_{TI} and V_{TO}. In most cases, a successful test is conducted with initial values: 2810, $V_m = -5$; 2401, $V_m = -1$; 2451, $V_{gg} = -10$; 3400, $V_{gg} = -10$. In some instances, it is necessary to slew the voltage from a region outside of the window and define V_T as the first voltage for which the data of all addresses is correct.

To measure a device when the programmed pattern is not known, or upon erasing or writing all zeros, a pattern of zeros or all ones must be used for the read comparison. A pattern of all ones will measure the maximum negative threshold of the array. A pattern of all zeros will measure the minimum negative threshold of the array. This pattern is used for the endurance predictive test.

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